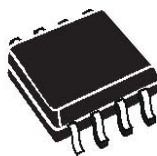


## Transition-mode PFC controller

### Features:

- Proprietary multiplier design for minimum THD
- Very accurate adjustable output overvoltage protection
- Ultra-low (30  $\mu$  A) Start-up current
- Low (2.5mA) quiescent current
- Digital leading-edge blanking on current sense
- Disable function on E/A input
- 1% (@  $T_J = 25^\circ\text{C}$ ) internal reference voltage
- -600/+800mA totem pole gate driver with active pull-down during UVLO and voltage clamp
- DIP-8/SO-8 packages



### Applications

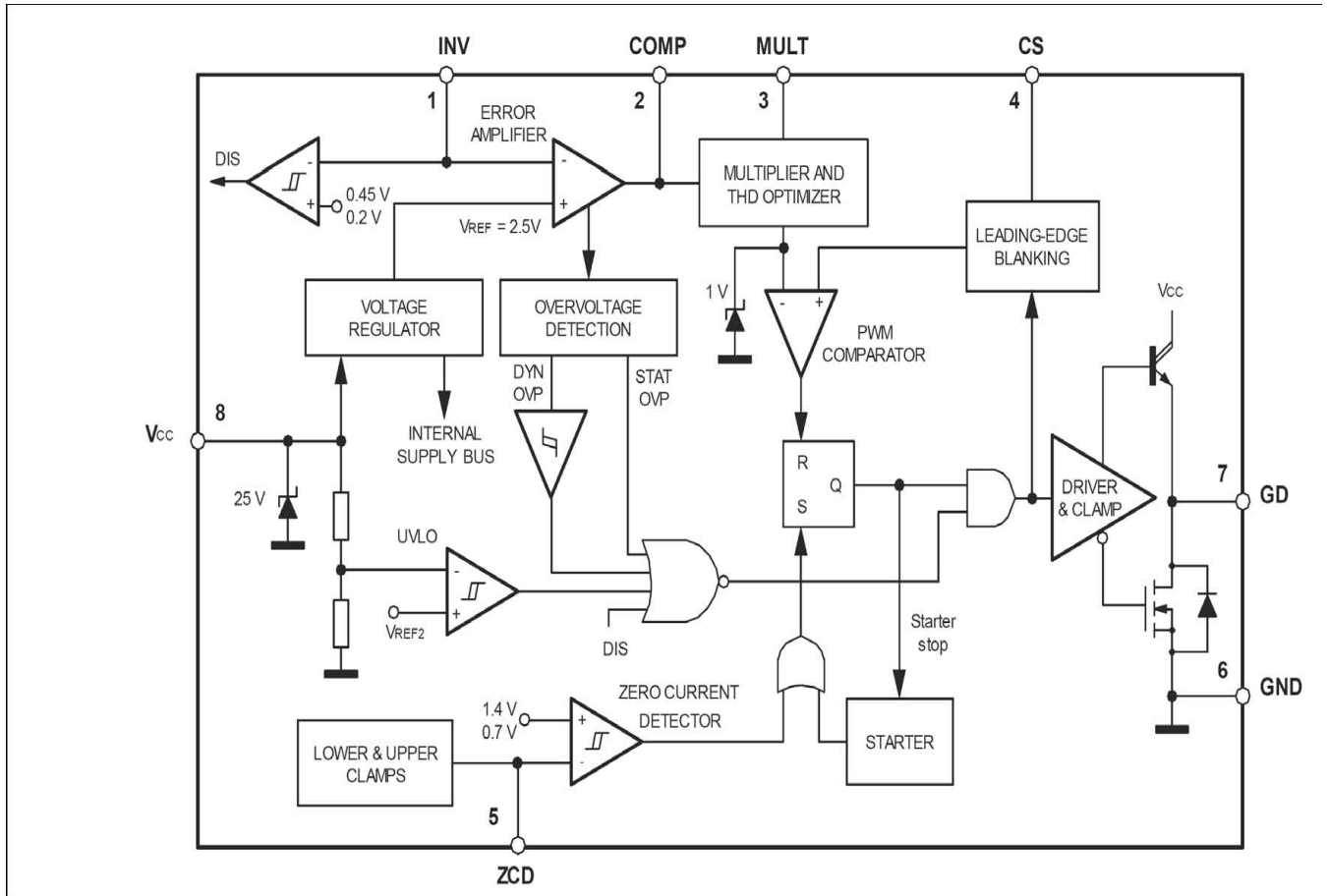
PFC pre-regulators for:

- IEC61000-3-2 compliant SMPS (Flat TV, monitors, desktop PC, games)
- HI-END AC-DC adapter/charger up to 400W
- Electronic ballast
- Entry level server & web server
- HI-END AC-DC adapter/charger up to 400W
- Electronic ballast
- Entry level server & web server

### Description

- The SC6562A is a current-mode PFC controller operating in Transition Mode (TM).
- The highly linear multiplier includes a special circuit, able to reduce AC input current distortion, that allows wide-range-mains operation with an extremely low THD, even over a large load range.
- The output voltage is controlled by means of a voltage-mode error amplifier and an accurate (1% @  $T_J = 25^\circ\text{C}$ ) internal voltage reference.
- The device features extremely low consumption (60 $\mu$ A max. before start-up and <5 mA operating) and includes a disable function suitable for IC remote ON/OFF, which makes it easier to comply with energy saving requirements (Blue Angel, EnergyStar, Energy2000, etc.).
- An effective two-step OVP enables to safely handle overvoltages either occurring at start-up or resulting from load disconnection.
- The totem-pole output stage, capable of 600 mA source and 800 mA sink current, is suitable to drive high current MOSFETs or IGBTs. This, combined with the other features and the possibility to operate with the proprietary Fixed-Off-Time control, makes the device

**Figure 1. Block diagram**

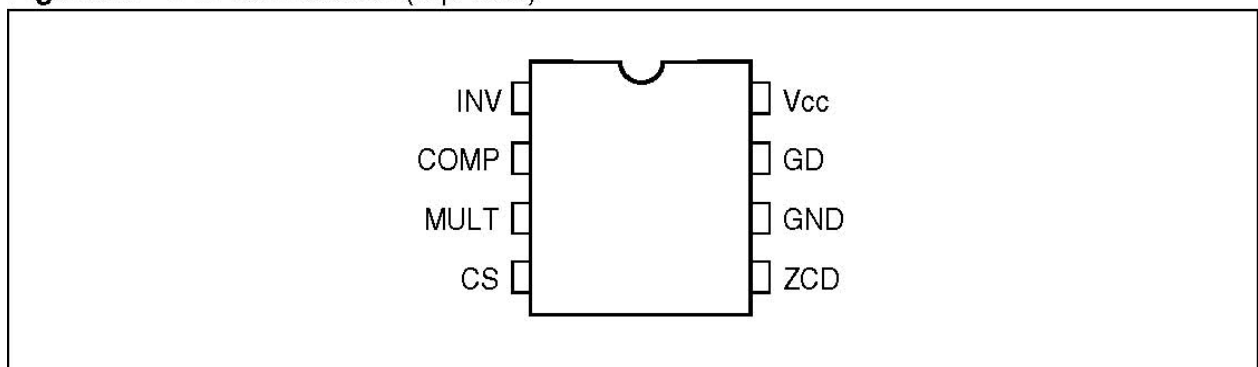


**Table 1. Device summary**

Order codes	Package	Packaging
SC6562AN	DIP-8	Tube
SC6562AD	SO-8	Tube
SC6562ADTR	SO-8	Tape & Reel

## Pin connection

**Figure 2. Pin connection (top view)**



## Pin description

**Table 2. Pin description**

Pin N°	Name	Description
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into this pin through a resistor divider. The pin doubles as an ON/OFF control input.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine MOSFET's turn-off. The pin is equipped with 200 ns leading-edge blanking for improved noise immunity.
5	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
6	GND	Ground. Current return for both the signal part of the IC and the gate driver.
7	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12V to avoid excessive gate voltages in case the pin is supplied with a high Vcc.
8	Vcc	Supply Voltage of both the signal part of the IC and the gate driver. The supply voltage upper limit is extended to 22V min. to provide more headroom for supply voltage changes.

## Maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Pin	Parameter	Unit	Unit
VCC	8	IC supply voltage( $I_{CC} \leq 20mA$ )	Self-limited	V
IGD	7	I Output totem pole peak current	Self-limited	A
---	1 to 4	Analog inputs & outputs	-0.3 to 8	V
IZCD	5	current detector max. current	$\pm 10$	mA

## Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Value		Unit
		SO8	DIP8	
RthJA	S Max. Thermal Resistance, Junction-toambient	150	100	°C/W
PTOT	Power Dissipation @TA = 50°C	0.65	1	W
TJ	Junction Temperature Operating range	-40 to 150		°C
TSTG	Storage Temperature	-55 to 150		°C

## Electrical characteristics

**Table 5. Electrical characteristics**

(-25°C < T<sub>J</sub> < +125°C, V<sub>CC</sub> = 12V, C<sub>o</sub> = 1nF; unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Symbol Itage						
VCC	Operating range	After turn-on	10.5		22.5	V
VccOn	Turn-on threshold	(1)	11.7	12.5	13.3	V
VccOff	Turn-off threshold	(1)	9.5	10	10.5	V
Hys	Hysteresis		2.2		2.8	V
VZ	Zener Voltage	ICC = 20mA	22.5	25	28	V
Supply current						
Istart-up	Start-up current	Before turn-on, VCC = 11V		30	60	μA
Iq	Quiescent current	After turn-on		2.5	3.75	mA
ICC	Operating supply current	@ 70kHz		3.5	5	mA
Iq	Quiescent current	During OVP (either static or dynamic) or VINV ≤150mV		1.7	2.2	v
Multiplier input						
IMULT	Input bias current	VMULT = 0 to 4V			-1	μA
VMULT	Linear operation range		0 to 3			V
$\frac{\Delta Vcs}{\Delta VMULT}$	Output max. slope	VMULT = 0 to 1V, VCOMP = Upper clamp	1	1.1		V/V
K	Gain (2)	VMULT = 1V, VCOMP= 4V,	0.32	0.38	0.44	v
Error amplifier						
VINV	Voltage feedback input threshold	TJ = 25 °C	2.475	2.5	2.525	V
		10.5V < VCC < 22.5V (1)	2.455		2.545	
	Line regulation	VCC = 10.5V to 22.5V		2	5	mV
IINV	Input bias current	VINV = 0 to 3V			-1	μA
Gv	Voltage gain	Open loop	60	80		dB
GB	Gain-bandwidth product			1		MHz
ICOMP	Source current	VCOMP = 4V, VINV = 2.4V	-2	-3.5	-5	mV
	Sink current	VCOMP = 4V, VINV = 2.6V	2.5	4.5		mV
VCOMP	Upper clamp voltage	ISOURCE = 0.5mA	5.3	5.7	6	V
	Lower clamp voltage	ISINK = 0.5mA (1)	2.1	2.25	2.4	V
VINVdis	Disable threshold		150	200	250	mV
VINVen	Restart threshold		380	450	520	mV
Output overvoltage						
IOVP	Dynamic OVP triggering current		23.5	27	30.5	μA
Hys	Hysteresis	(3)		20		μA
	Static OVP threshold	(1)	2.1	2.25	2.4	V
Current sense comparator						
ICS	Input bias current	VCS = 0			-1	μA
tLEB	Leading edge blanking		100	200	300	ns
td(H-L)	Delay to output			175		ns
VCS	Current sense clamp	VCOMP = Upper clamp, Vmult = 1.5V	1.0	1.08	1.16	V
Vcsoffset	Current sense offset	VMULT = 0		25		mV
		VMULT = 2.5V		5		
Zero current detector						
VZCDH	Upper clamp voltage	IZCD = 2.5mA	5.0	5.7	6.5	V
VZCDL	Lower clamp voltage	IZCD = - 2.5mA	-0.3	0	0.3	V
VZCDA	Arming voltage (positive-going edge)	(3)		1.4		V
VZCDT	Triggering voltage (negative-going edge)	(3)		0.7		V
IZCDb	Input bias current	VZCD = 1 to 4.5V		2		μA
IZCDsrc	Source current capability		-2.5			mA
IZCDsnk	Sink current capability		2.5			mA
Starter						
tSTART	Start timer period		75	190	300	us

Gate driver						
VOL	Output low voltage	Isink = 100mA		0.6	1.2	V
VOH	Output high voltage	Isource = 5mA	9.8	10.3		V
Isrcpk	Peak source current		-0.6			A
Isnkpk	Peak sink current		0.8			A
tf	Voltage fall time			30	70	ns
tr	Voltage rise time			60	110	ns
VOclamp	Output clamp voltage	Isource = 5mA; Vcc = 20 V	10	12	15	V
	UVLO saturation	Vcc = 0 to VCCCon, Isink = 2 mA			1.1	V

1. All the parameters are in tracking
2. The multiplier output is given by:
3. Parameters guaranteed by design, functionality tested in production.

## Typical electrical characteristic

Figure 3. Supply current vs supply voltage

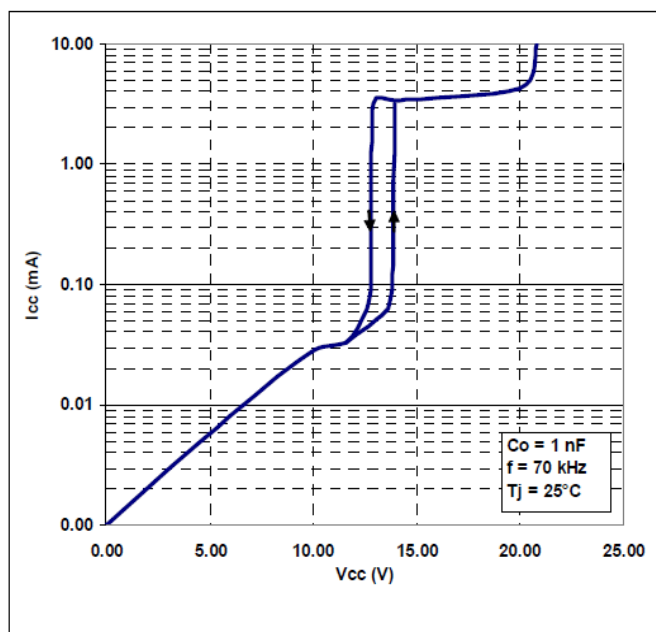
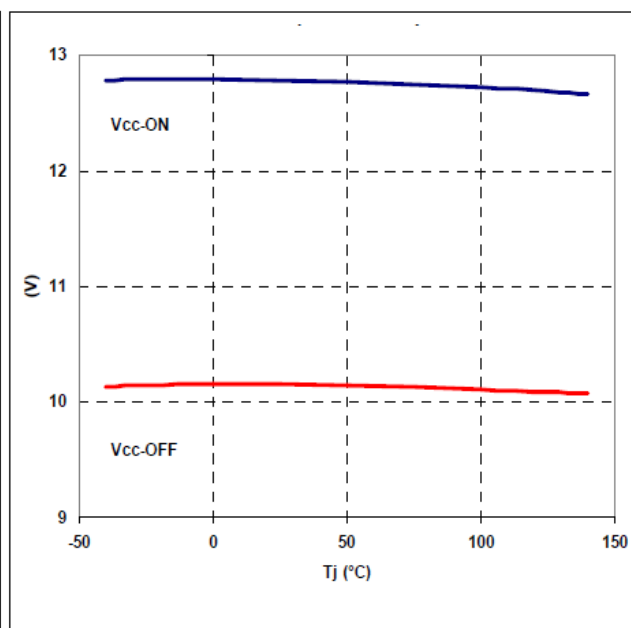
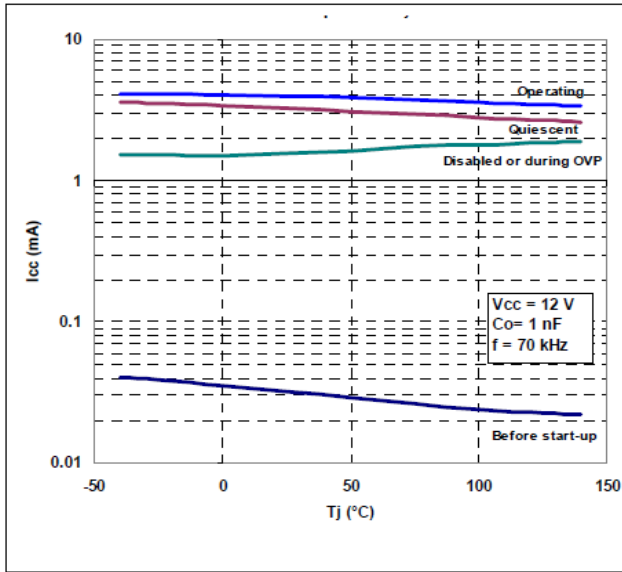


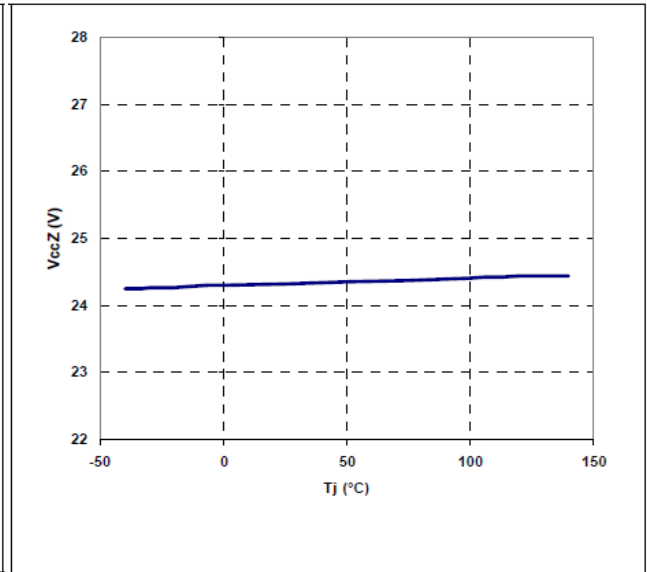
Figure 4. Start-up & UVLO vs TJ



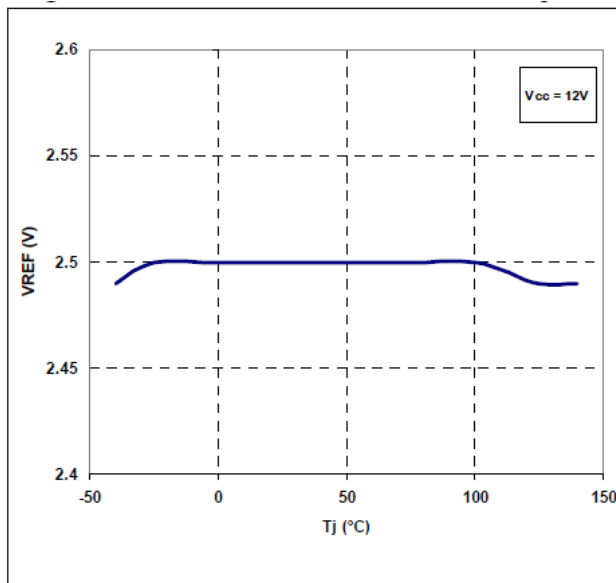
**Figure 5. IC consumption vs TJ**



**Figure 6. Vcc Zener voltage vs TJ**



**Figure 7. Feedback reference vs TJ**



**Figure 8. OVP current vs TJ**

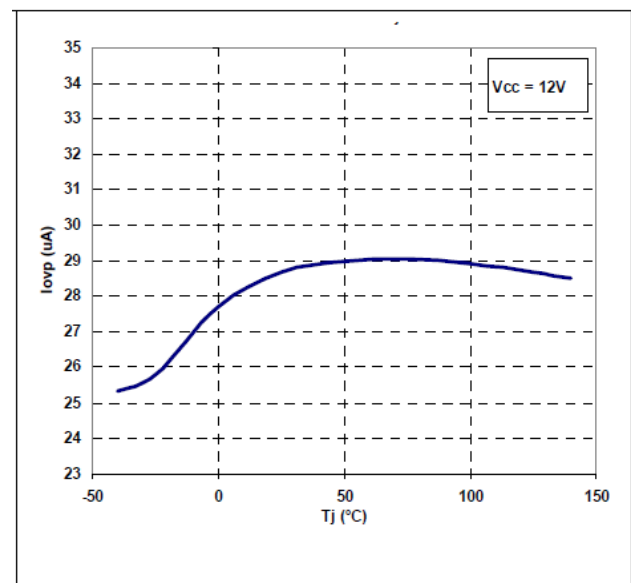


Figure 9. E/A output clamp levels vs TJ

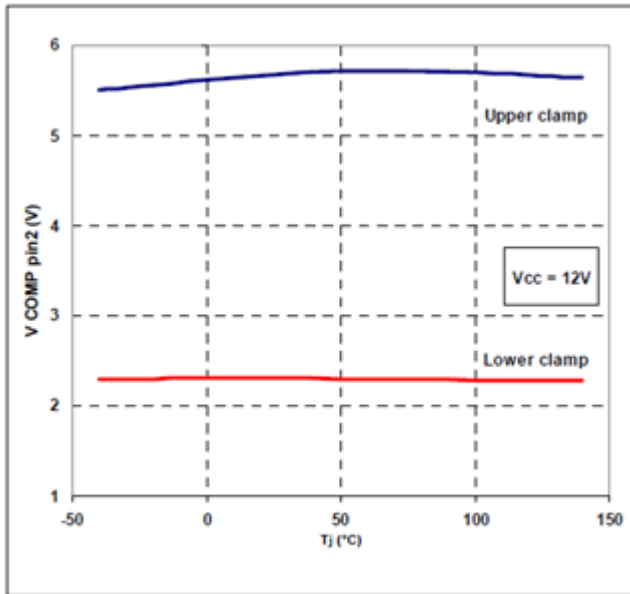


Figure 10. Delay-to-output vs TJ

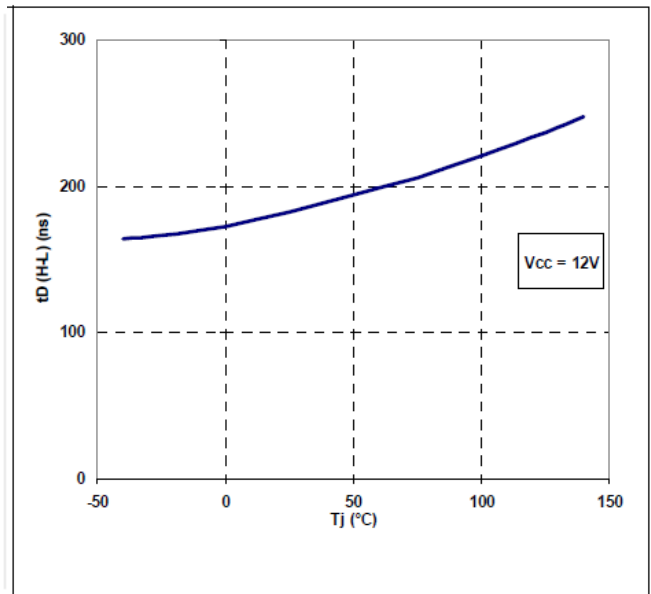


Figure 11. Multiplier characteristic

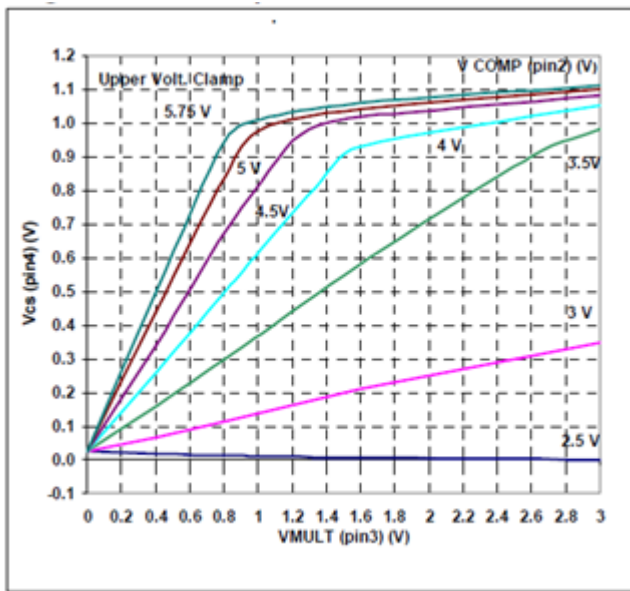
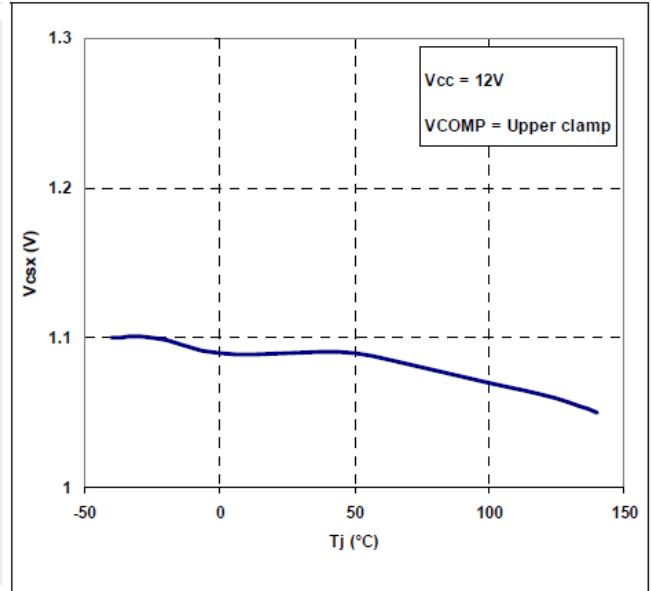
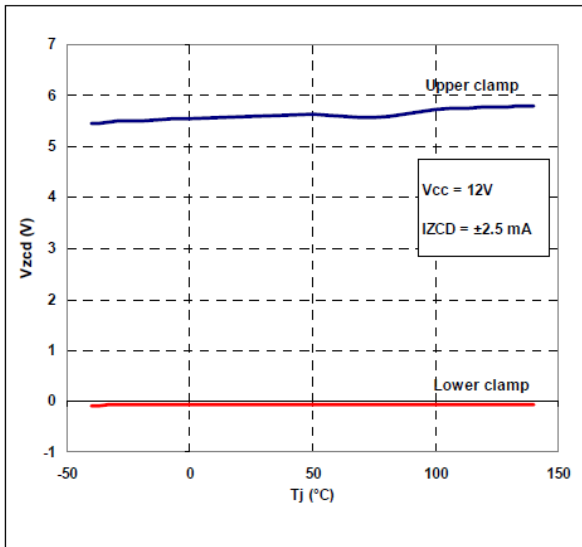


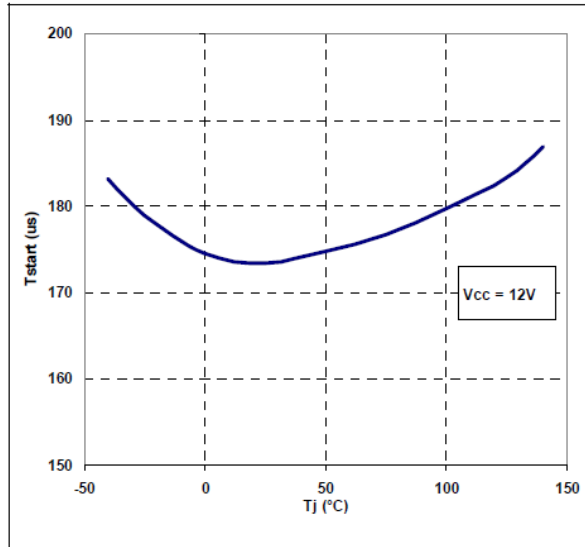
Figure 12. Vcs clamp vs TJ



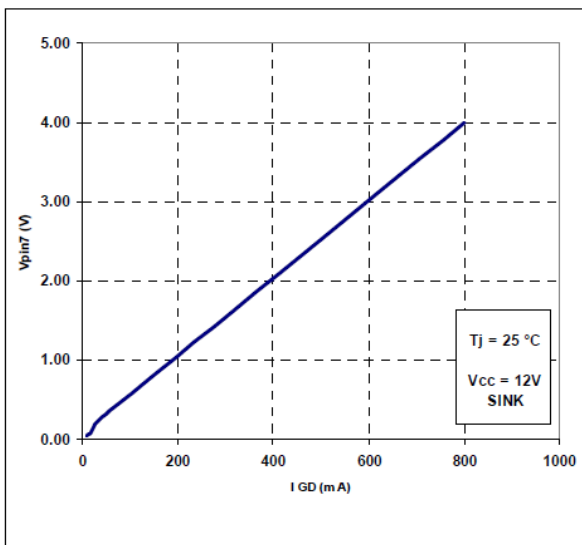
**Figure 13. ZCD clamp levels vs TJ**



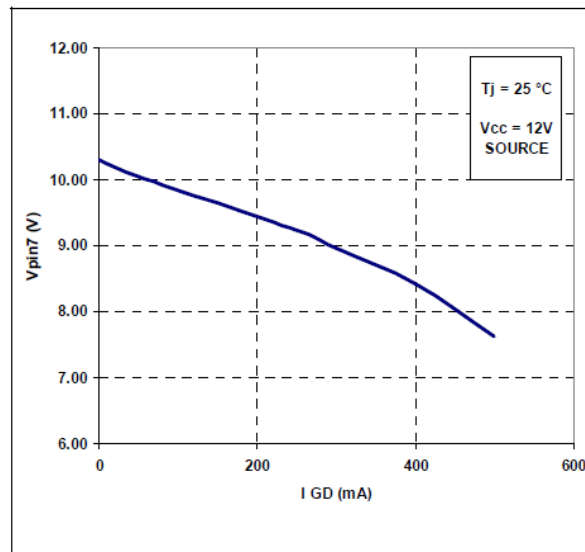
**Figure 14. Start-up timer vs TJ**



**Figure 15. Gate-driver output low Saturation**

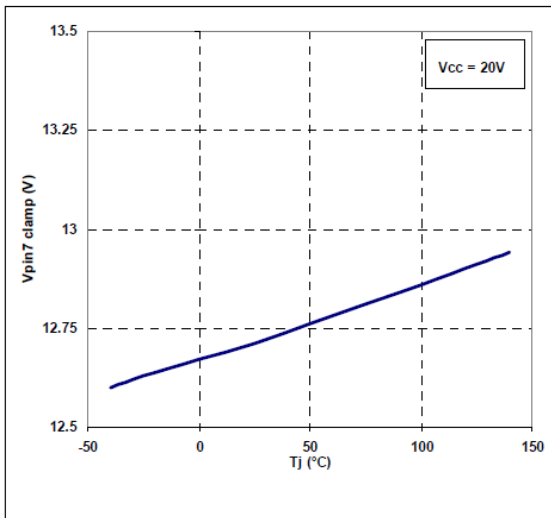


**Figure 16. Gate-drive output high saturation**

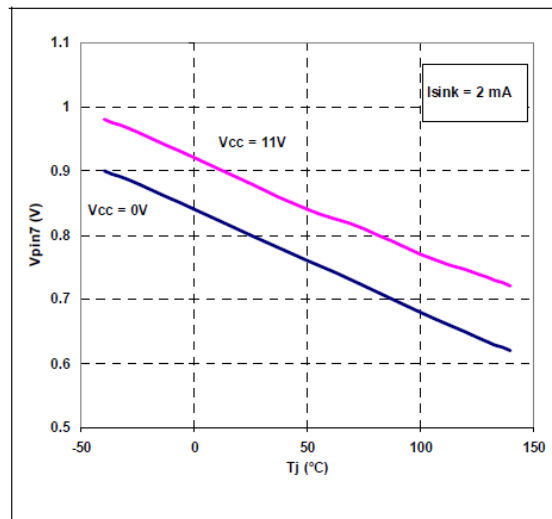




**Figure 17. Gate-drive clamp vs TJ**



**Figure 18. Output gate drive low saturation vs TJ during UVLO**



## Application information

### Overvoltage protection

Under steady-state conditions, the voltage control loop keeps the output voltage  $V_o$  of a PFC pre-regulator close to its nominal value, set by the resistors  $R_1$  and  $R_2$  of the output divider. Neglecting ripple components, the current through  $R_1$ ,  $I_{R1}$ , equals that through  $R_2$ ,  $I_{R2}$ . Considering that the non-inverting input of the error amplifier is internally referenced at 2.5V, also the voltage at pin INV will be 2.5V, then:

#### Equation 1

$$I_{R2} = I_{R1} = \frac{2.5}{R2} = \frac{V_o - 2.5}{R1}$$

If the output voltage experiences an abrupt change  $\Delta V_o > 0$  due to a load drop, the voltage at pin INV will be kept at 2.5V by the local feedback of the error amplifier, a network connected between pins INV and COMP that introduces a long time constant to achieve high PF (this is why  $\Delta V_o$  can be large). As a result, the current through  $R_2$  will remain equal to  $2.5/R_2$  but that through  $R_1$  will become:

## Equation 2

$$I'_{R1} = \frac{V_O - 2.5 + \Delta V_O}{R1}$$

The difference current  $\Delta I_{R1} = I'_{R1} - I_{R2} = I'_{R1} - I_{R1} = \Delta V_O / R1$  will flow through the compensation network and enter the error amplifier output (pin COMP). This current is monitored inside the device and if it reaches about 24μA the output voltage of the multiplier is forced to decrease, thus smoothly reducing the energy delivered to the output. As the current exceeds 27μA, the OVP is triggered (Dynamic OVP): the gate-drive is forced low to switch off the external power transistor and the IC put in an idle state. This condition is maintained until the current falls below approximately 7μA, which re-enables the internal starter and allows switching to restart. The output  $\Delta V_O$  that is able to trigger the Dynamic OVP function is then:

## Equation 3

$$\Delta V_O = R1 \cdot 20 \cdot 10^{-6}$$

An important advantage of this technique is that the OV level can be set independently of the regulated output voltage: the latter depends on the ratio of R1 to R2, the former on the individual value of R1. Another advantage is the precision: the tolerance of the detection current is 13%, i.e. 13% tolerance on  $\Delta V_O$ . Since  $\Delta V_O \ll V_O$ , the tolerance on the absolute value will be proportionally reduced.

Example:  $V_O = 400V$ ,  $\Delta V_O = 40V$ . Then:  $R1 = 40V / 27\mu A \approx 1.5M\Omega$  ;  
 $R2 = 1.5M\Omega \cdot 2.5 / (400 - 2.5) = 9.43k\Omega$ . The tolerance on the OVP level due to the SC6562A will be  $40 \cdot 0.13 = 5.3V$ , that is  $\pm 1.2\%$ .

## Application information

When the load of a PFC pre-regulator is very low, the output voltage tends to stay steadily above the nominal value, which cannot be handled by the Dynamic OVP. If this occurs, however, the error amplifier output will saturate low; hence, when this is detected the external power transistor is switched off and the IC put in an idle state (Static OVP). Normal operation is resumed as the error amplifier goes back into its linear region. As a result, the device will work in burst-mode, with a repetition rate that can be very low.

When either OVP is activated the quiescent consumption of the IC is reduced to minimize the discharge of the Vcc capacitor and increase the hold-up capability of the IC supply system.

## Disable function

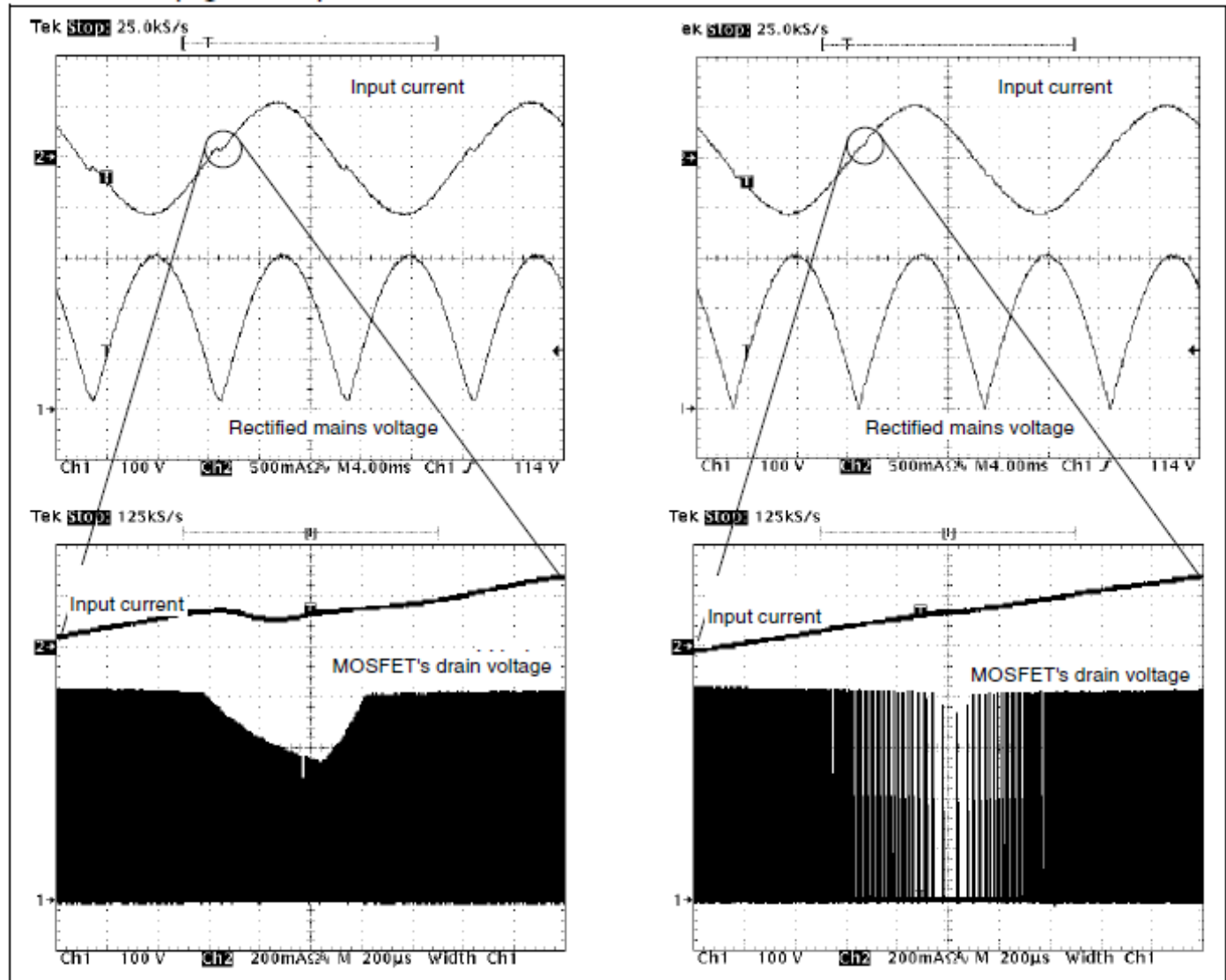
The INV pin doubles its function as a not-latched IC disable: a voltage below 0.2V shuts down the IC and reduces its consumption at a lower value. To restart the IC, the voltage on the pin must exceed 0.45 V. The main usage of this function is a remote ON/OFF control input that can be driven by a PWM controller for power management purposes. However it also offers a certain degree of additional safety since it will cause the IC to shutdown in case the lower resistor of the output divider is shorted to ground or if the upper resistor is missing or fails open.

### **THD optimizer circuit**

The device is equipped with a special circuit that reduces the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way the THD (Total Harmonic Distortion) of the current is considerably reduced.

A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the highfrequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

**Figure 19. THD optimization: standard TM PFC controller (left side) and SC6562A (right side)**



To overcome this issue the circuit embedded in the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This will result in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge. The effect of the circuit is shown in figure 2, where the key waveforms of a standard TM PFC controller are compared to those of the SC6562A.

Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid.

To maximally benefit from the THD optimizer circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized, compatibly with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself - even with an ideal energy transfer by the PFC pre-regulator - thus making the action of the

optimizer circuit little effective.

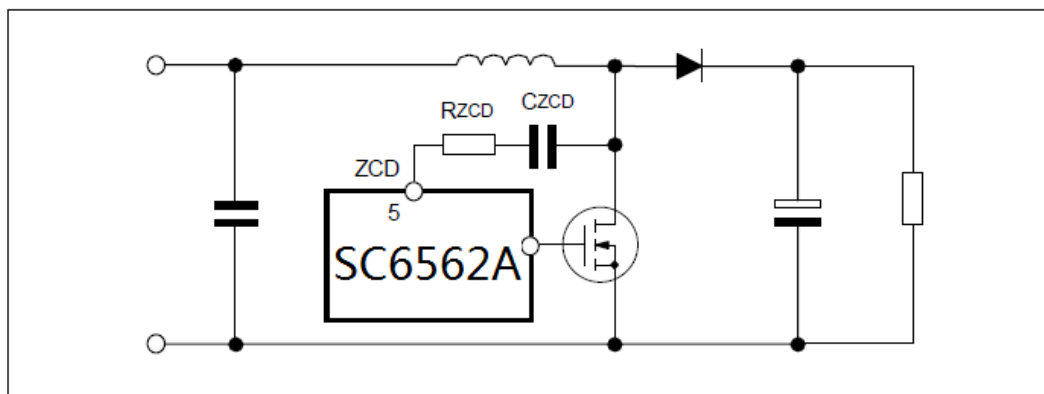
## Operating with no auxiliary winding on the boost inductor

To generate the synchronization signal on the ZCD pin, the typical approach requires the connection between the pin and an auxiliary winding of the boost inductor through a limiting resistor. When the device is supplied by the cascaded DC-DC converter, it is necessary to introduce a supplementary winding to the PFC choke just to operate the ZCD pin.

Another solution could be implemented by simply connecting the ZCD pin to the drain of the power MOSFET through an R-C network as shown in figure 3: in this way the highfrequency edges experienced by the drain will be transferred to the ZCD pin, hence arming and triggering the ZCD comparator.

Also in this case the resistance value must be properly chosen to limit the current sourced/sunk by the ZCD pin. In typical applications with output voltages around 400V, recommended values for these components are 22pF (or 33pF) for CZCD and 330k for RZCD. With these values proper operation is guaranteed even with few volts difference between the regulated output voltage and the peak input voltage

**Figure 20. ZCD pin synchronization without auxiliary winding**



## Application examples and ideas

Figure 21. Demo board TM-80W, wide-range mains : electrical schematic

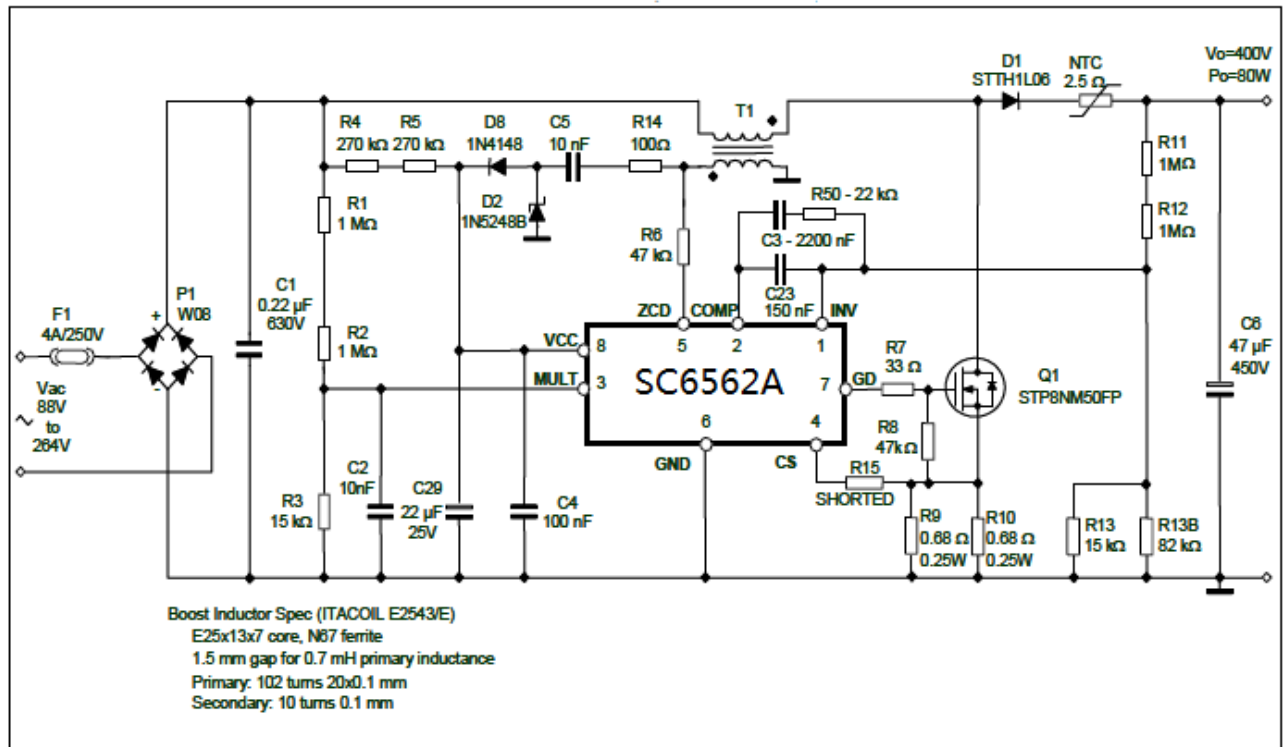


Figure 22. SC6562A 80W TM PFC evaluation board: compliance to EN61000-3-2 standard

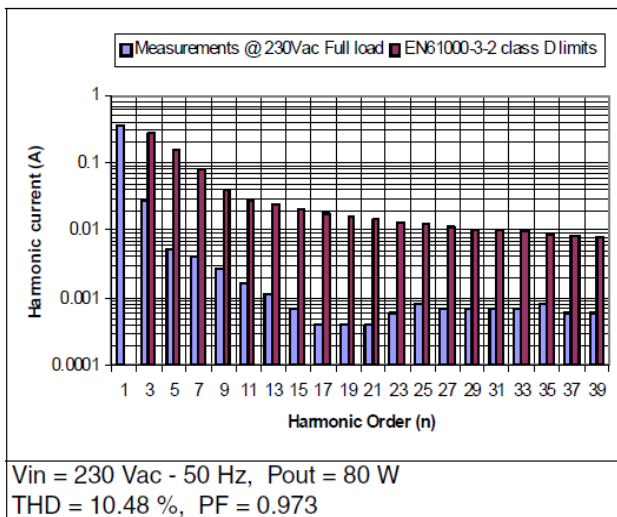
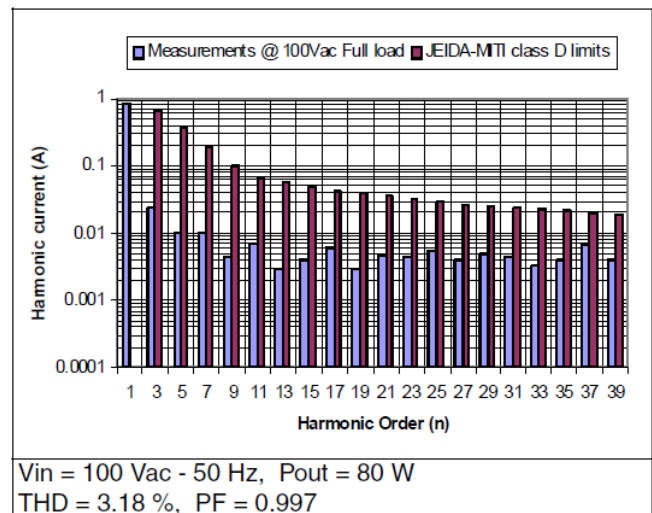
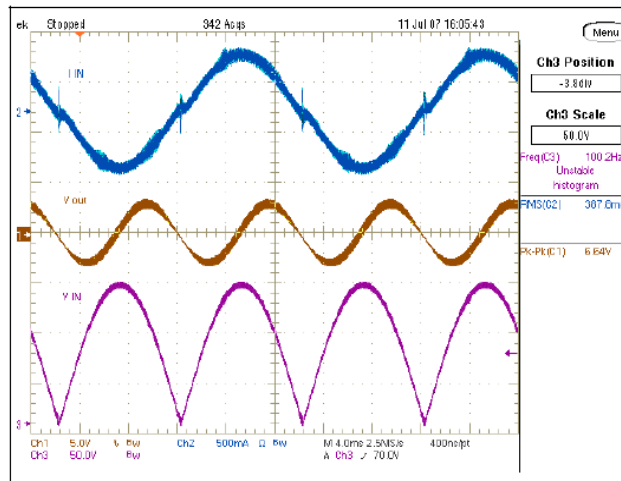


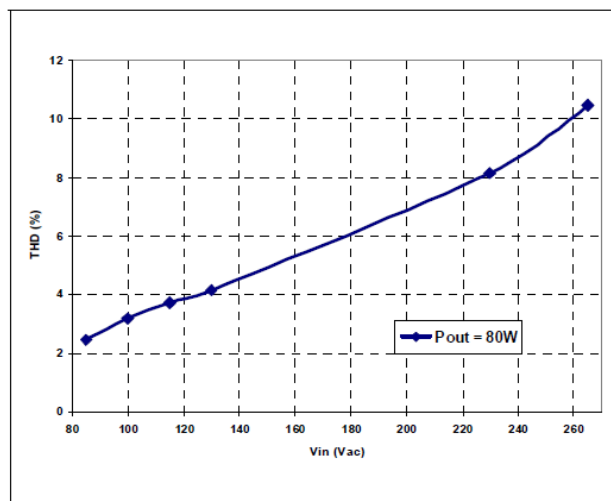
Figure 23. SC6562A 80W TM PFC evaluation board: compliance to JEIDA-MITI standard



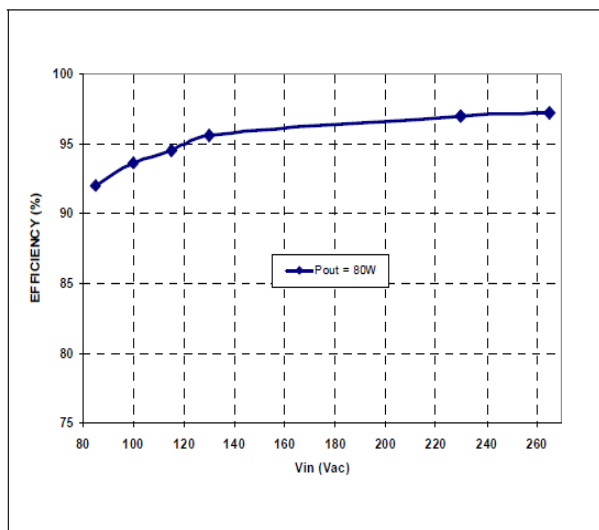
**Figure 25. Figure 4- SC6562A 80W TM PFC  
Evaluation board: Input Current  
waveform @100V-50Hz – 80W load**



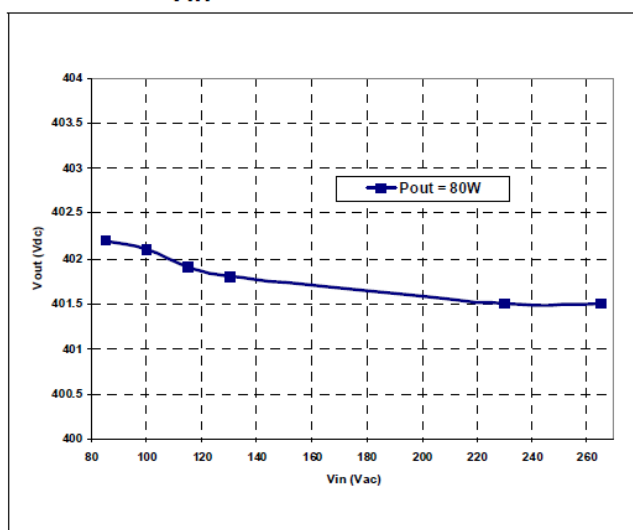
**Figure 27. SC6562A 80W TM PFC evaluation  
board: THD vs Vin**



**Figure 28. SC6562A 80W TM PFC evaluation  
board: efficiency vs**



**Figure 29. SC6562A 80W TM PFC Evaluation  
Vinboard: Static Vout regulation vs  
Vin**

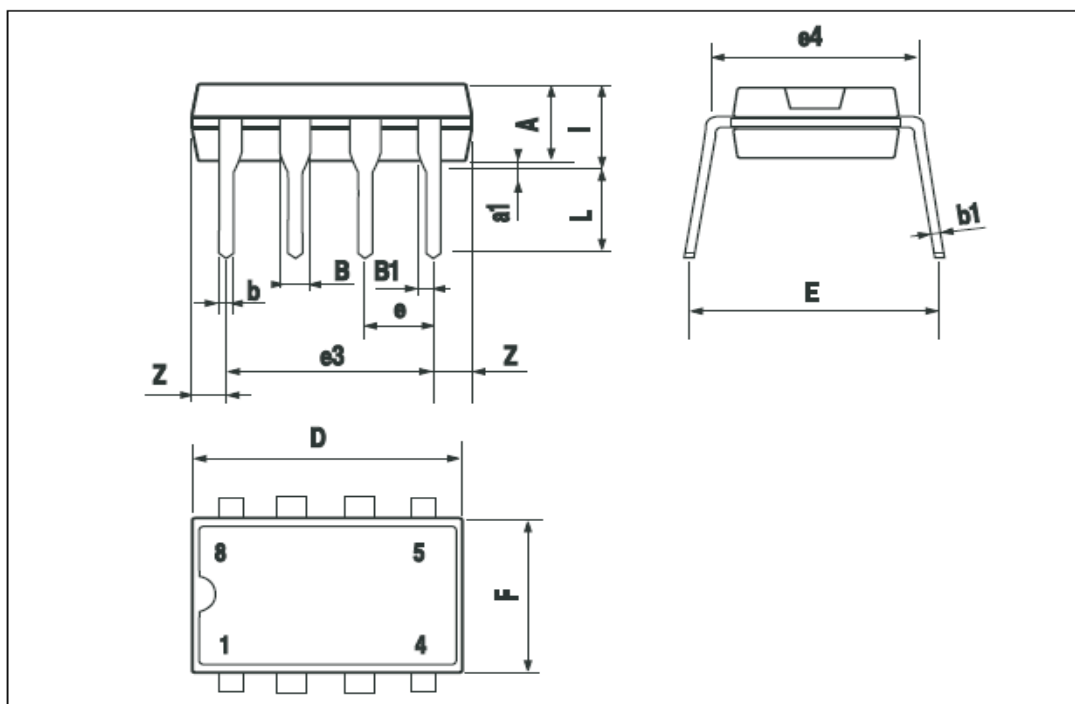




Dim.	mm			Inch		
	Min	Typ	Max	Min	Typ	Max
A		3.32			0.131	
a1	0.51			0.020		

B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

**Figure 31. Package dimensions**

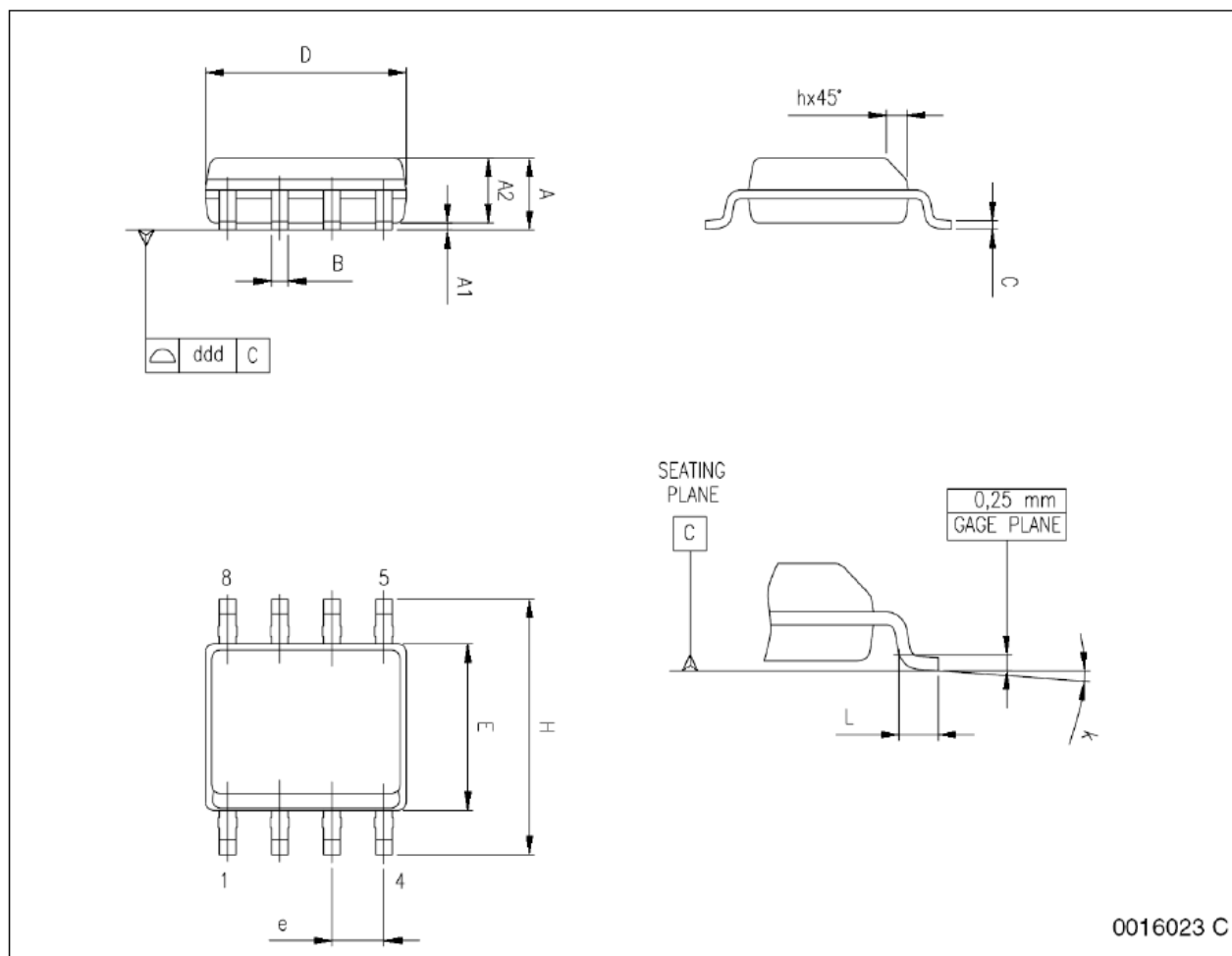


**Table 8. SO-8 mechanical data**

Dim.	mm			Inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

**Figure 32. Package dimensions**



## CONTACT INFORMATION

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