



600V N-ch Planar MOSFET

Lead Free Package and Finish

General Features

- RoHS Compliant
- $R_{DS(ON),typ.}=0.65\ \Omega @ V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

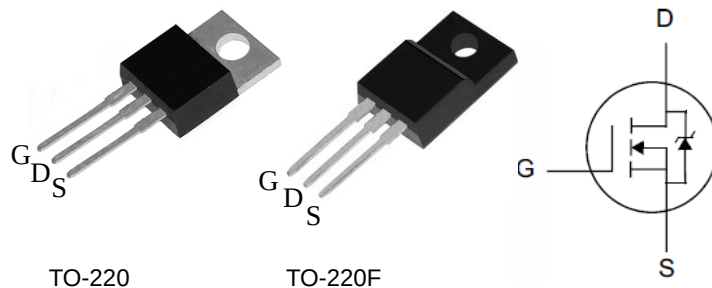
BV_{DSS}	$R_{DS(ON),typ.}$	I_D
600V	0.65Ω	10A

Applications

- Adaptor
- Charger
- SMPS Standby Power

Ordering Information

Part Number	Package	Brand
KR10N60C	TO-220	KR
KR10N60FC	TO-220F	KR



Package No to Scale

Absolute Maximum Ratings

$T_C=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	KR10N60C	KR10N60FC	Unit
V _{DSS}	Drain-to-Source Voltage	600		V
V _{GSS}	Gate-to-Source Voltage	±30		
I _D	Continuous Drain Current	10		A
I _{DM}	Pulsed Drain Current at V _{GS} =10V	38		
E _{AS}	Single Pulse Avalanche Energy	700		mJ
P _D	Power Dissipation	125	69	W
	Derating Factor above 25°C	1.0	0.55	W/°C
T _L	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300		°C
T _J & T _{STG}	Operating and Storage Temperature Range	-55 to 150		

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	KR10N60C	KR10N60FC	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.0	1.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	100	



Electrical Characteristics

OFF Characteristics

 $T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	600	--	--	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	$V_{DS}=600V, V_{GS}=0V$
		--	--	100		$V_{DS}=480V, V_{GS}=0V, T_J=125^{\circ}\text{C}$
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	$V_{GS}=+30V, V_{DS}=0V$
		--	--	-100		$V_{GS}=-30V, V_{DS}=0V$

ON Characteristics

 $T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	0.65	0.75	Ω	$V_{GS}=10V, I_D=5.0A$
$V_{GS(TH)}$	Gate Threshold Voltage	3.0	--	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
gfs	Forward Transconductance	--	5.0	--	S	$V_{DS}=15V, I_D=5.0A$

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	1264	1700	pF	$V_{GS}=0V, V_{DS}=25V, f=1.0MHz$
C_{rss}	Reverse Transfer Capacitance	--	18	26		
C_{oss}	Output Capacitance	--	149	200		
Q_g	Total Gate Charge	--	31	46	nC	$V_{DD}=480V, I_D=10A, V_{GS}=0 \text{ to } 10V$
Q_{gs}	Gate-to-Source Charge	--	5.5	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	18	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	23	55	nS	$V_{DD}=300V, I_D=10A, V_{GS}=10V, R_g=25\Omega$
t_{rise}	Rise Time	--	69	150		
$t_{d(OFF)}$	Turn-Off Delay Time	--	144	300		
t_{fall}	Fall Time	--	77	165		

**Source-Drain Body Diode Characteristics** $T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current ^[2]	--	--	10	A	Integral pn-diode in MOSFET
I_{SM}	Pulsed Source Current ^[2]	--	--	38		
V_{SD}	Diode Forward Voltage	--	--	1.5	V	$I_S=10\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	--	420	--	ns	$V_{GS}=0\text{V}$ $I_F=I_S$, $di/dt=100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovery Charge	--	4.2	--	μC	

Note:[1] $T_J=+25^{\circ}\text{C}$ to $+150^{\circ}\text{C}$ [2] Pulse width $\leq 380\mu\text{s}$; duty cycle $\leq 2\%$.



Typical Characteristics

Figure 1. Output Characteristics ($T_J = 25^\circ\text{C}$)

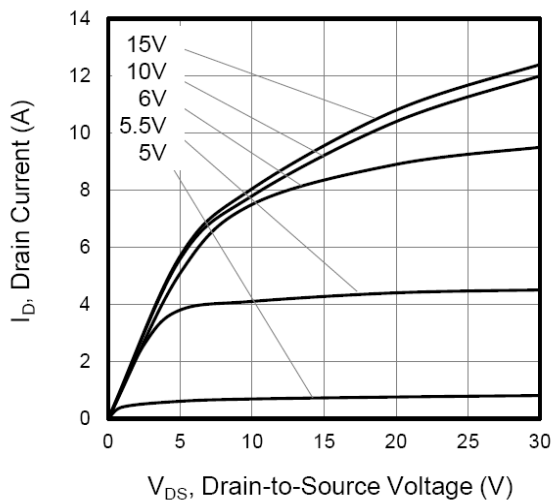


Figure 2. Forward Bias Safe Operating Area

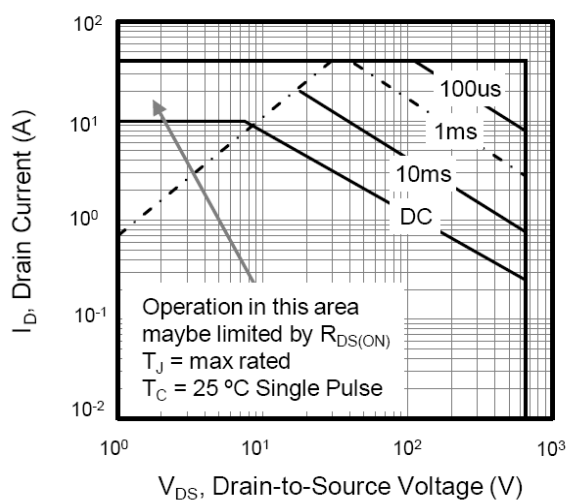


Figure 3. Drain Current vs. Temperature

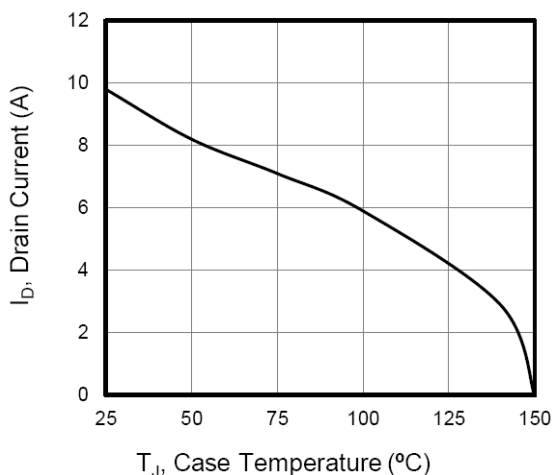


Figure 4. BV_{DSS} Variation vs. Temperature

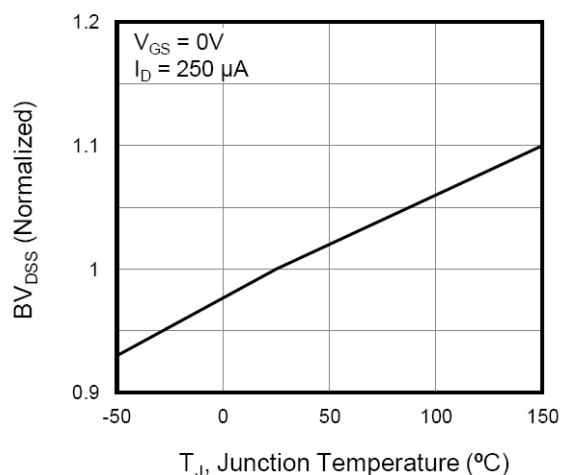


Figure 5. Transfer Characteristics

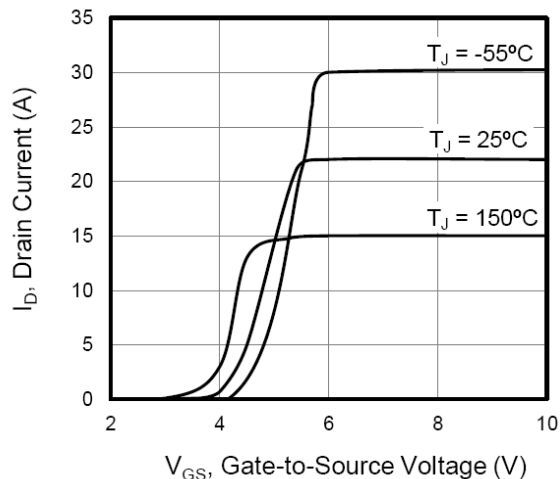
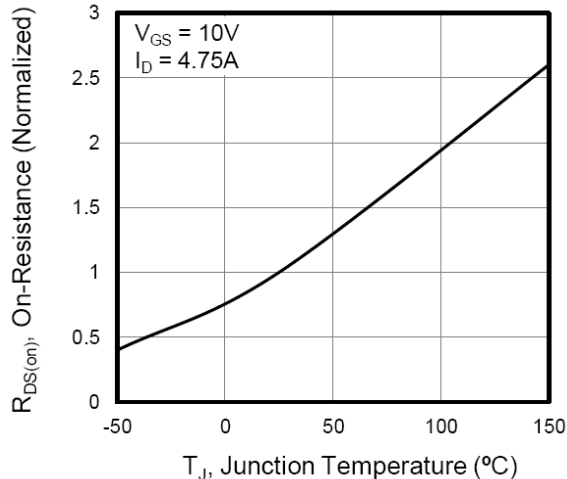


Figure 6. On-Resistance vs. Temperature





Typical Characteristics(Cont.)

Figure 7. Capacitance

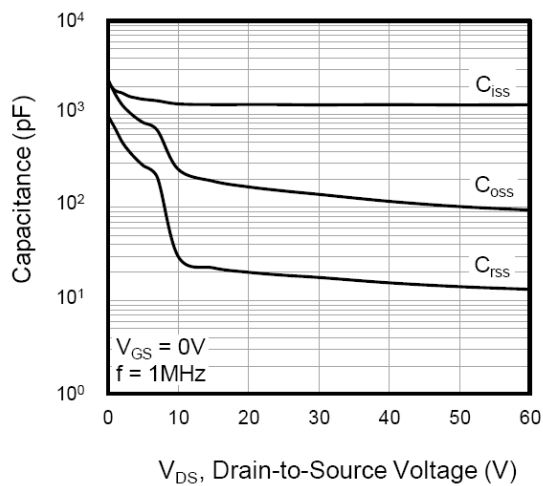


Figure 8. Gate Charge

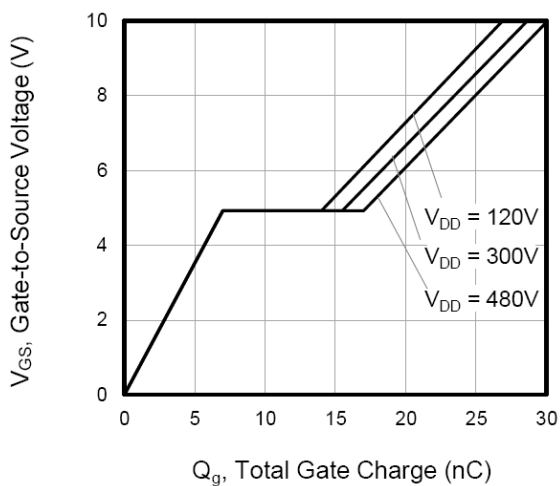


Figure 9. Body Diode Forward Voltage

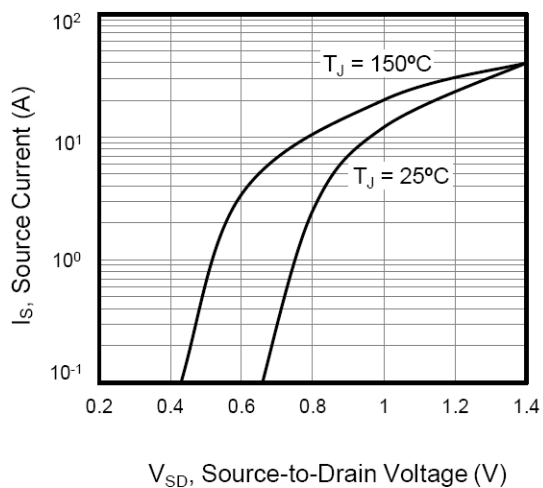
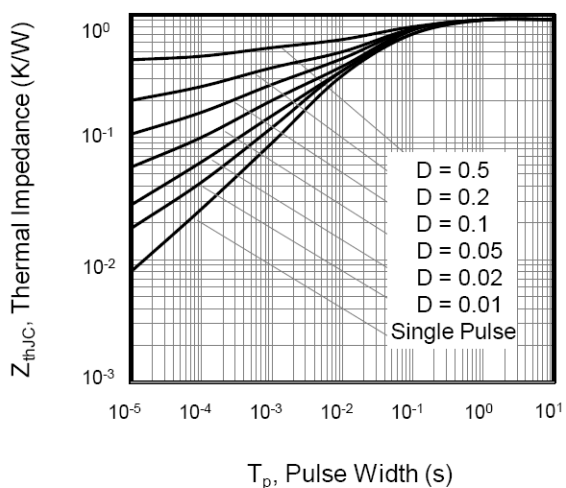


Figure 10. Transient Thermal Impedance





Test Circuits and Waveforms

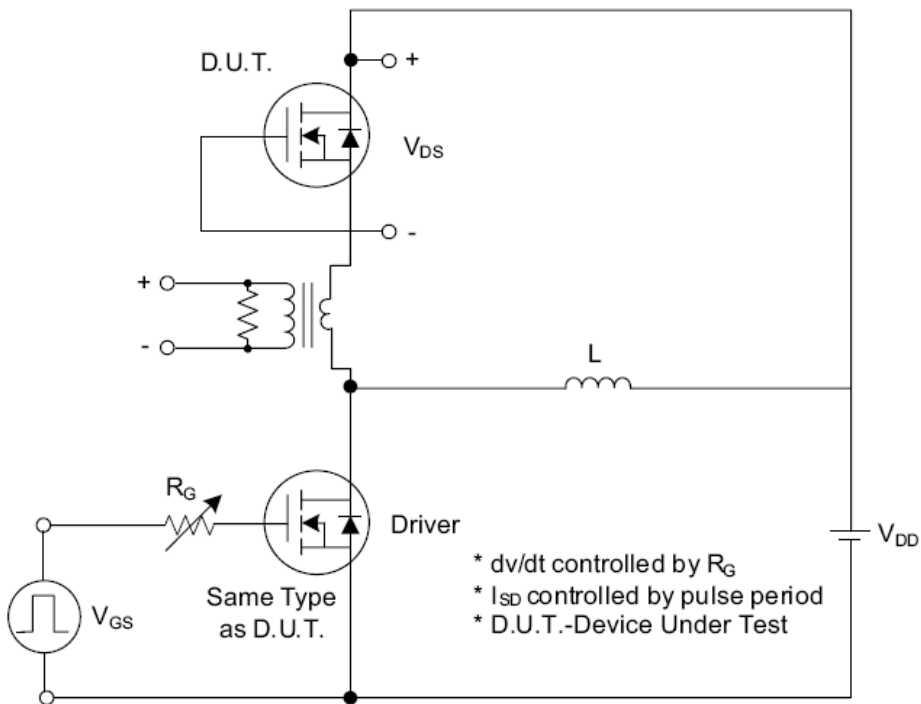


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

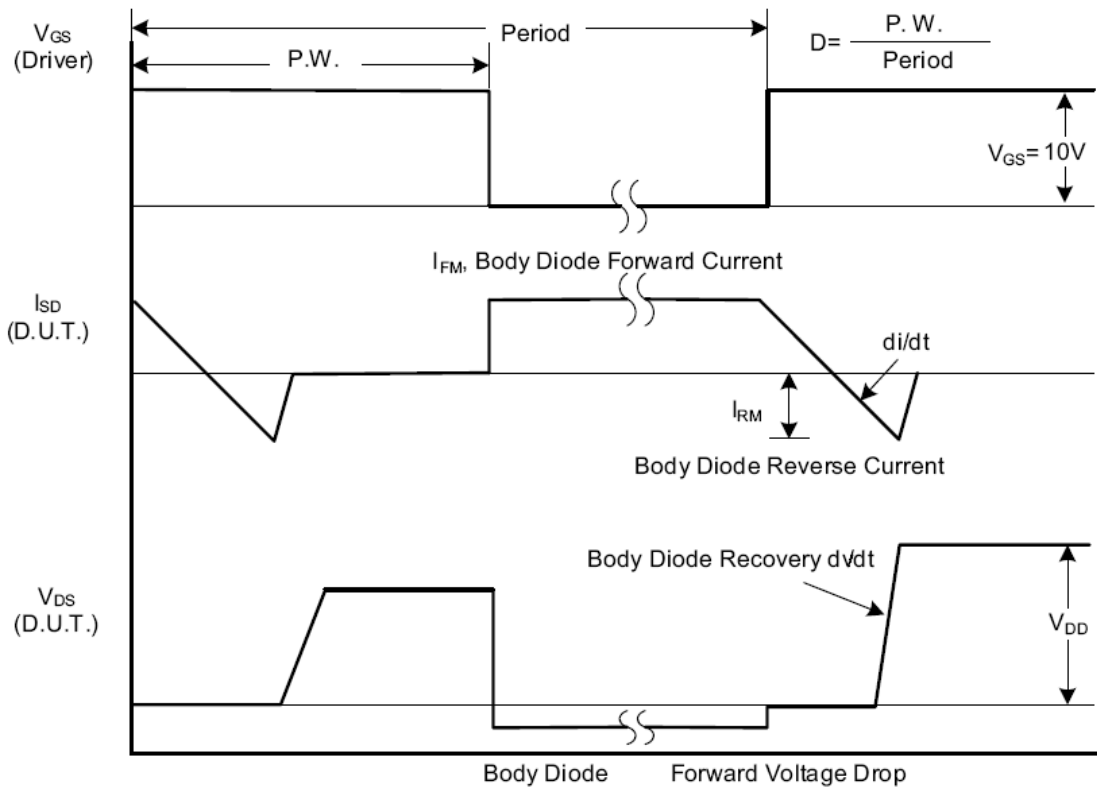


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms



Test Circuits and Waveforms (Cont.)

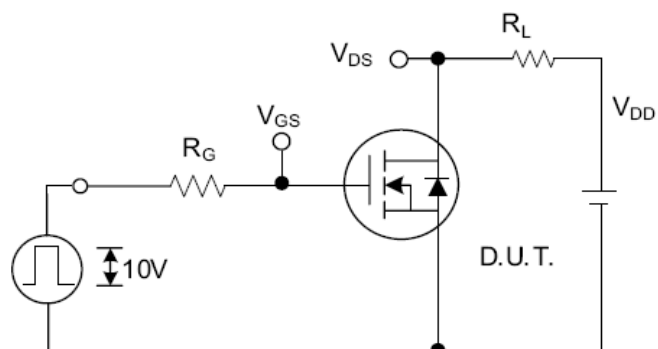


Fig. 2.1 Switching Test Circuit

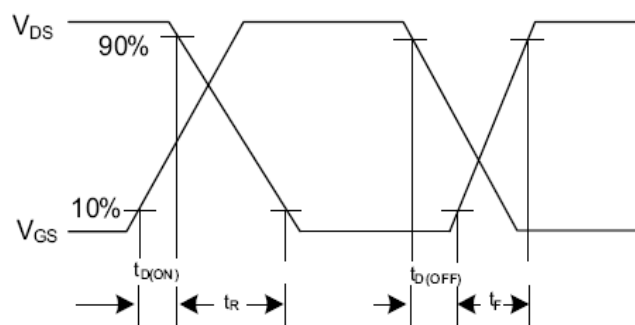


Fig. 2.2 Switching Waveforms

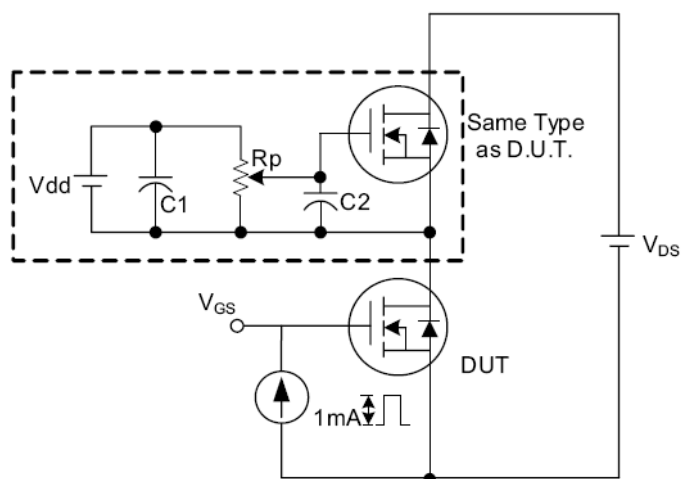


Fig. 3.1 Gate Charge Test Circuit

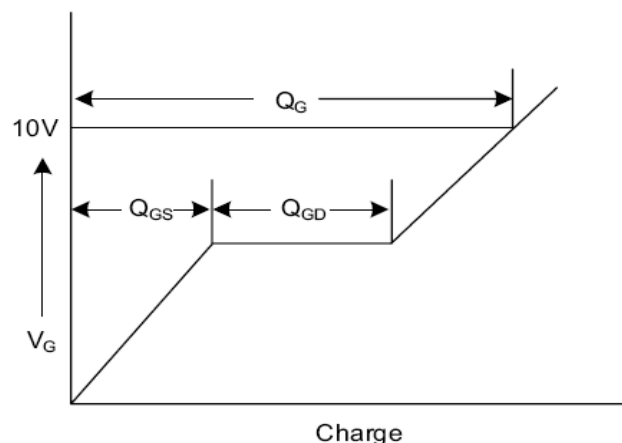


Fig. 3.2 Gate Charge Waveform

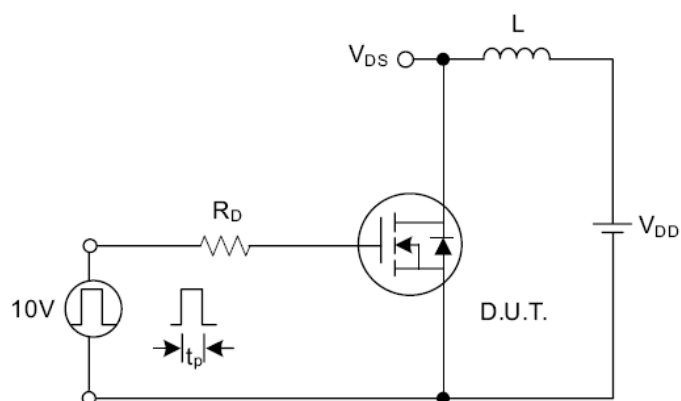


Fig. 4.1 Unclamped Inductive Switching Test Circuit

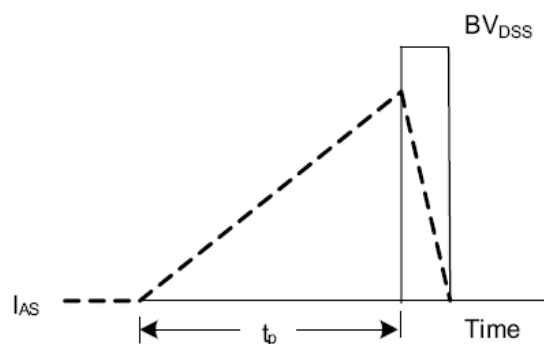


Fig. 4.2 Unclamped Inductive Switching Waveforms