650V N-ch Planar MOSFET

Lead Free Package and Finish

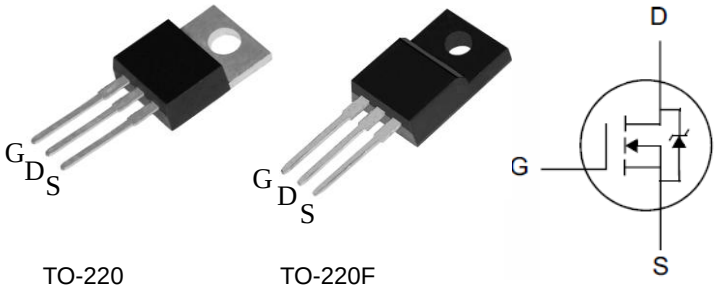
BV_{DSS}	$R_{DS(ON),typ.}$	I_D
650V	0.70Ω	10A

General Features

- RoHS Compliant
- $R_{DS(ON),typ.}$=0.70 Ω@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

Applications

- Adaptor
- Charger
- SMPS Standby Power



TO-220 TO-220F

Package No to Scale

Ordering Information

Part Number	Package	Brand
KR10N65C	TO-220	KR
KR10N65FC	TO-220F	KR

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	KR10N65C	KR10N65FC	Unit
V_{DSS}	Drain-to-Source Voltage	650		V
V_{GSS}	Gate-to-Source Voltage	±30		
I_D	Continuous Drain Current	10		A
I_{DM}	Pulsed Drain Current at V_{GS}=10V	38		
E_{AS}	Single Pulse Avalanche Energy	700		mJ
P_D	Power Dissipation	125	65	W
	Derating Factor above 25℃	1.0	0.52	W/℃
T_L	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300		℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150		

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	KR10N65C	KR10N65FC	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.0	1.92	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	100	

Electrical Characteristics

OFF Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	650	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=650V, V_{GS}=0V
		--	--	100		V_{DS}=520V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+30V, V_{DS}=0V
		--	--	-100		V_{GS}=-30V, V_{DS}=0V

ON Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	0.70	0.85	Ω	V_{GS}=10V, I_D=5.0A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA
gfs	Forward Transconductance	--	5.5	--	S	V_{DS}=15V,ID=5.0A

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	1340	--	pF	V_{GS}=0V, V_{DS}=25V, f=1.0MH_Z
C_{rss}	Reverse Transfer Capacitance	--	12	--		
C_{oss}	Output Capacitance	--	130	--		
Q_g	Total Gate Charge	--	43	--	nC	V_{DD}=480V, I_D=10A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	6.6	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	18	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	20	--	nS	V_{DD}=300V, I_D=10A, V_{GS}=10V Rg=25Ω
t_{rise}	Rise Time	--	70	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	134	--		
t_{fall}	Fall Time	--	75	--		

Source-Drain Body Diode Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current[2]	--	--	10	A	Integral pn-diode in MOSFET
I_{SM}	Pulsed Source Current[2]	--	--	38		
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_S=10A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	400	--	ns	V_{GS}=0V I_F= I_S, di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	4.0	--	uC	

Note:

[1] T_J=+25℃ to +150℃
[2] Pulse width≤380μs; duty cycle≤2%.

Typical Characteristics

Figure 1. Output Characteristics (T_J = 25ºC)

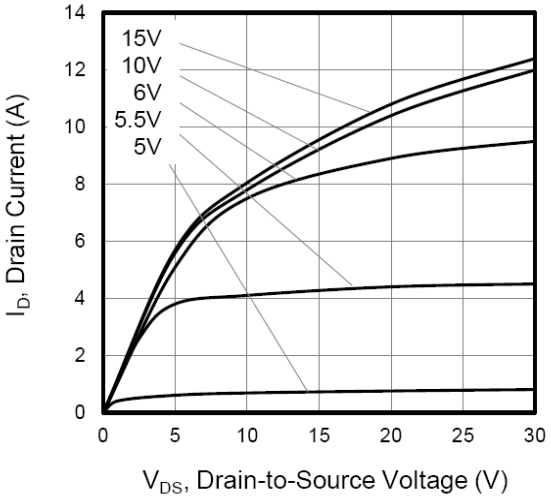


Figure 2. Forward Bias Safe Operating Area

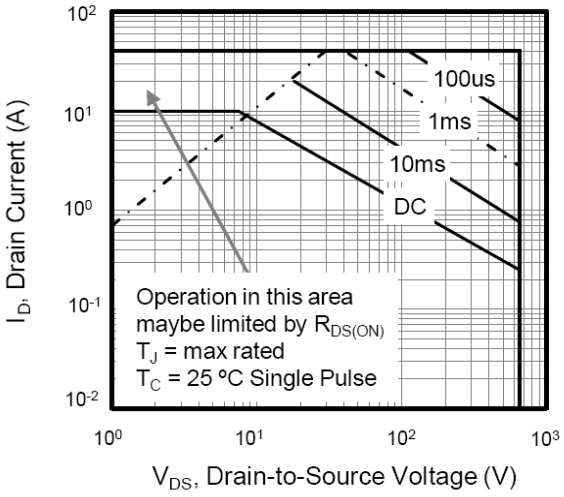


Figure 3. Drain Current vs. Temperature

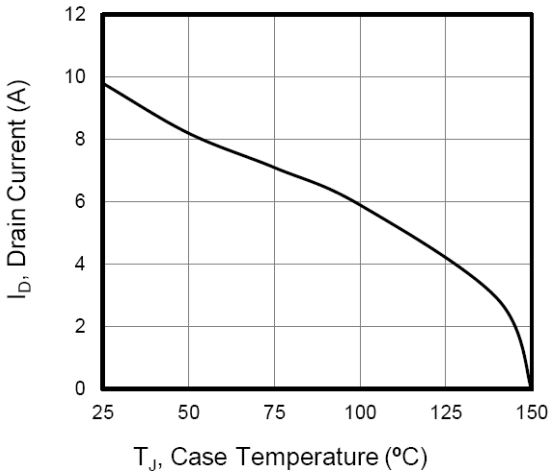
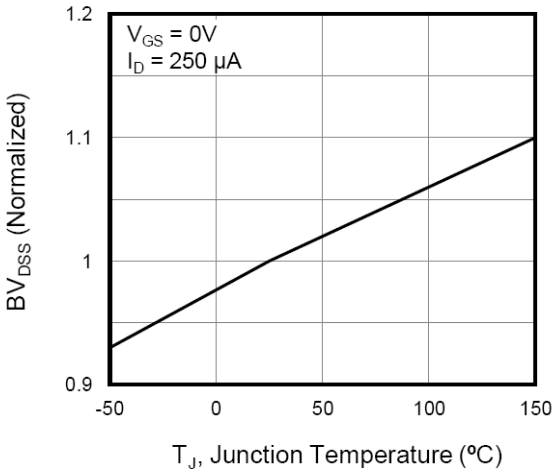


Figure 4. BV_{DSS} Variation vs. Temperature



Typical Characteristics(Cont.)

Figure 7. Capacitance

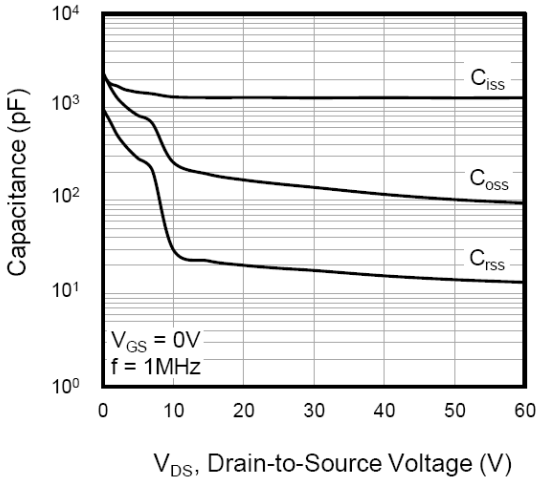


Figure 8. Gate Charge

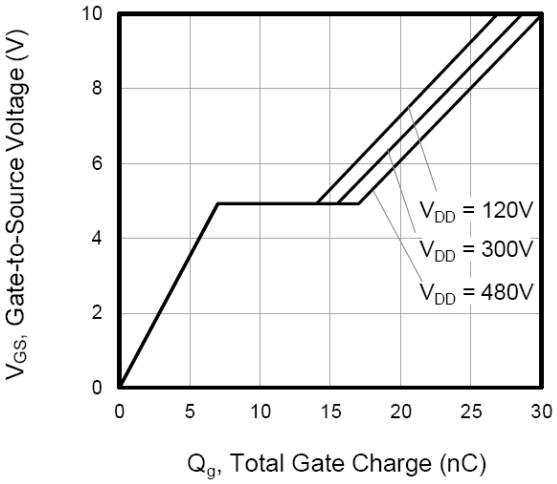


Figure 9. Body Diode Forward Voltage

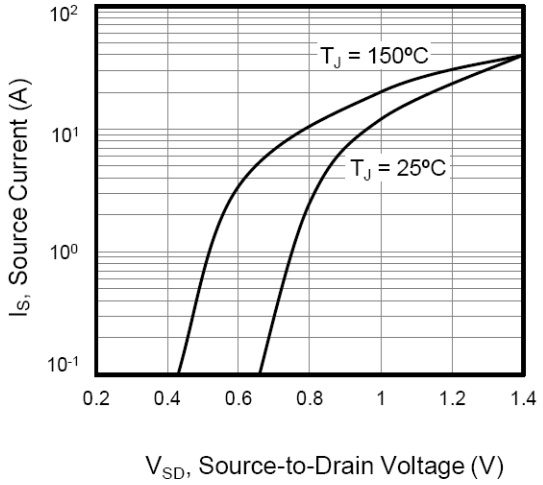
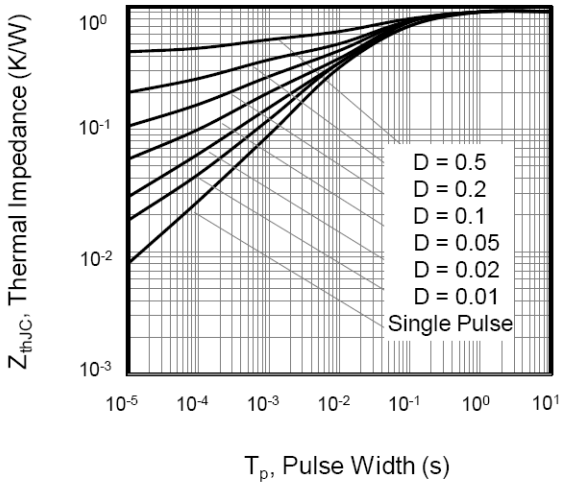


Figure 10. Transient Thermal Impedance



Test Circuits and Waveforms

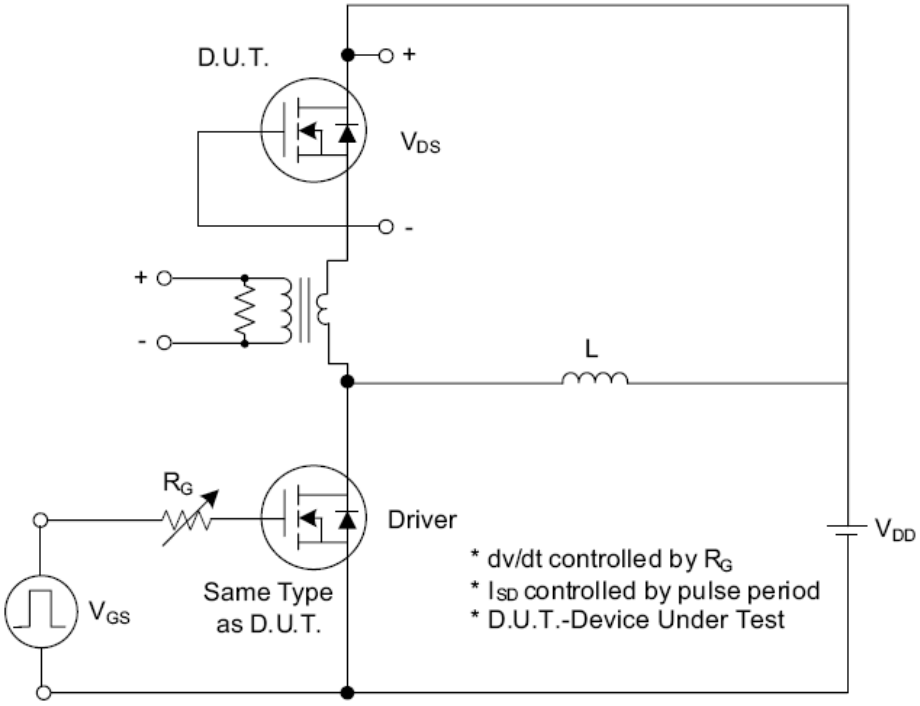


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

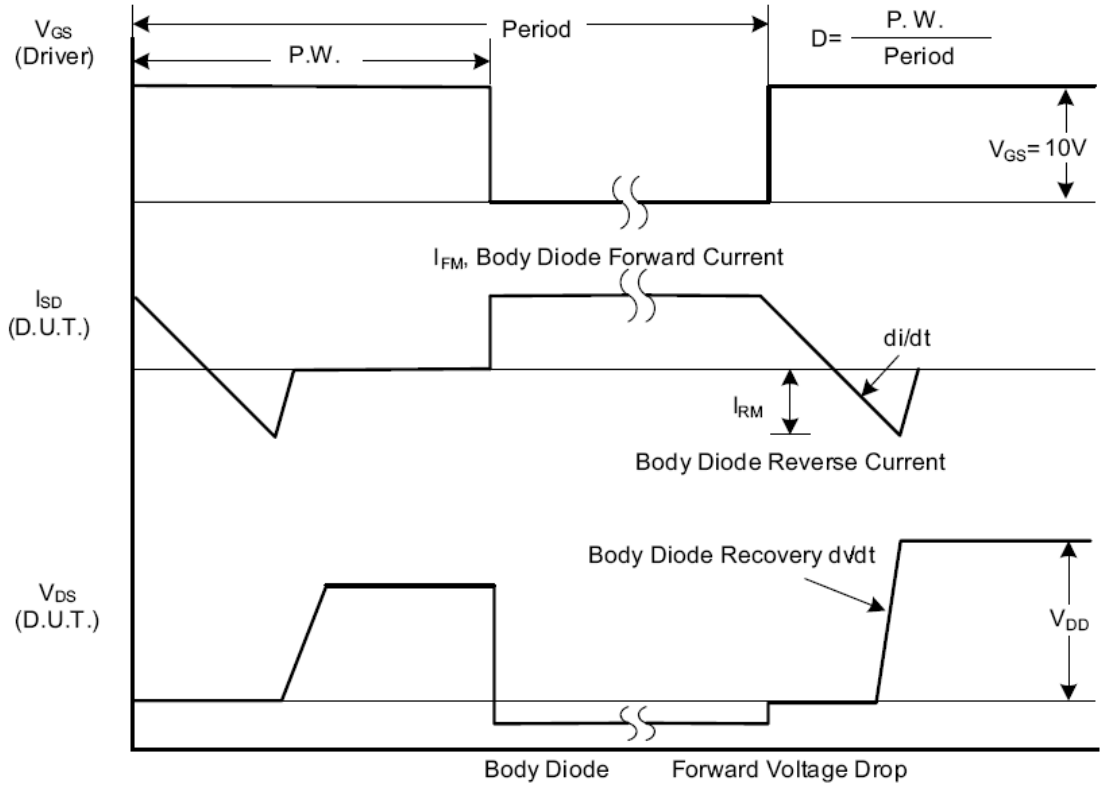


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

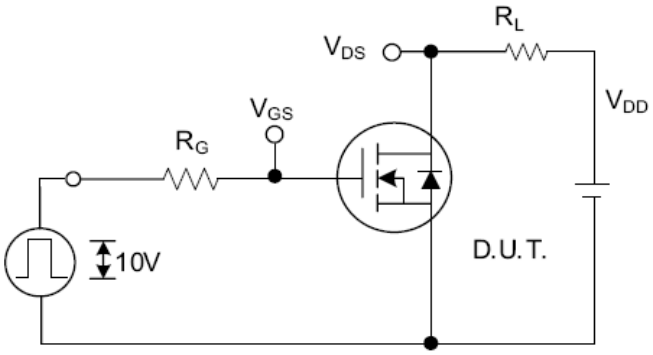


Fig. 2.1 Switching Test Circuit

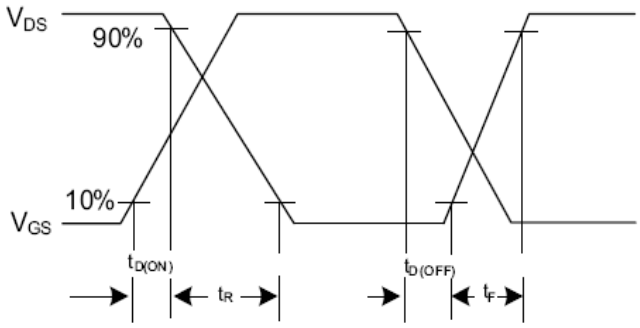


Fig. 2.2 Switching Waveforms

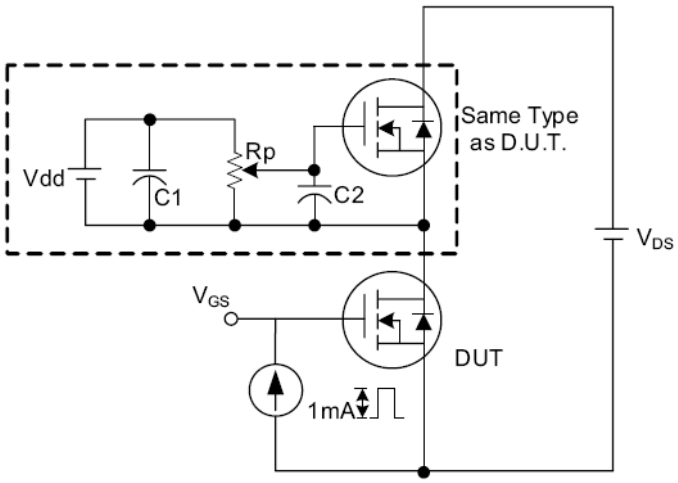


Fig. 3 . 1 Gate Charge Test Circuit

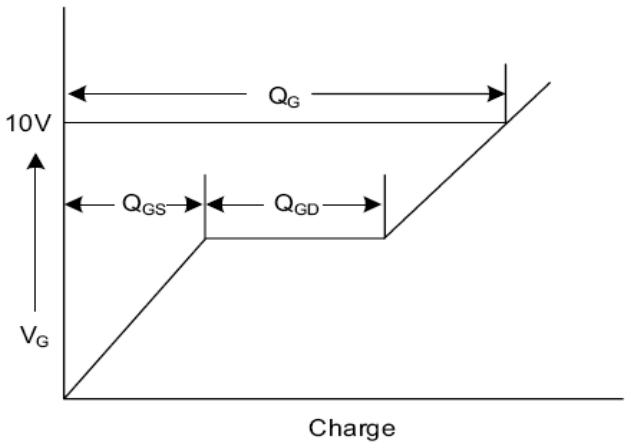


Fig. 3 . 2 Gate Charge Waveform

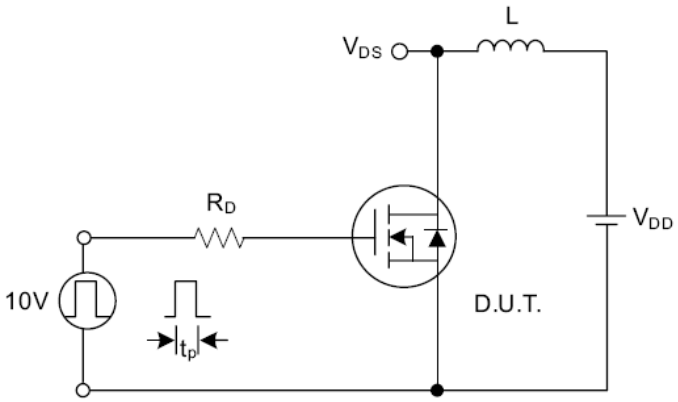


Fig. 4.1 Unclamped Inductive Switching Test Circuit

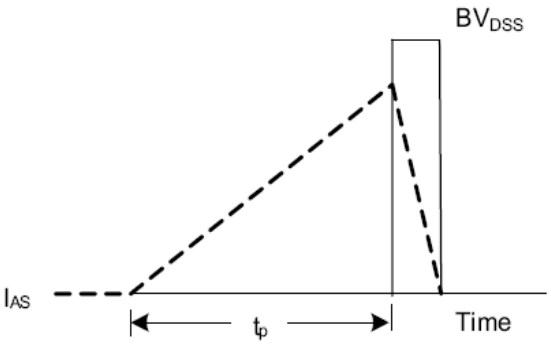


Fig. 4.2 Unclamped Inductive Switching Waveforms