



## 650V N-ch Planar MOSFET

Lead Free Package and Finish

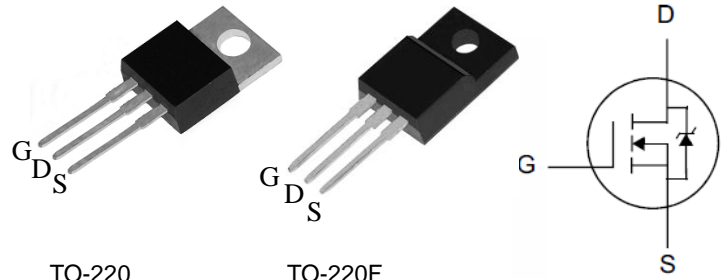
### General Features

- RoHS Compliant
- $R_{DS(ON),typ.}=0.60\ \Omega@V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

$BV_{DSS}$	$R_{DS(ON),typ.}$	$I_D$
650V	0.60Ω	12A

### Applications

- Adaptor
- Charger
- SMPS Standby Power



TO-220

TO-220F

Package No to Scale

### Ordering Information

Part Number	Package	Brand
KR12N65	TO-220	KR
KR12N65F	TO-220F	KR

### Absolute Maximum Ratings

$T_C=25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	KR12N65	KR12N65F	Unit
$V_{DSS}$	Drain-to-Source Voltage	650		V
$V_{GSS}$	Gate-to-Source Voltage	±30		
$I_D$	Continuous Drain Current	12		A
$I_{DM}$	Pulsed Drain Current at $V_{GS}=10V$	48		
$E_{AS}$	Single Pulse Avalanche Energy	450		mJ
$P_D$	Power Dissipation	125	73	W
	Derating Factor above 25°C	1.0	0.58	W/°C
$T_L$	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300		°C
$T_J \& T_{STG}$	Operating and Storage Temperature Range	-55 to 150		

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

### Thermal Characteristics

Symbol	Parameter	KR12N65	KR12N65F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.0	1.71	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	100	



## Electrical Characteristics

### OFF Characteristics

 $T_J = 25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	650	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	1	$\mu A$	$V_{DS}=650V, V_{GS}=0V$
		--	--	100		$V_{DS}=520V, V_{GS}=0V, T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Leakage Current	--	--	+100	$nA$	$V_{GS}=+30V, V_{DS}=0V$
		--	--	-100		$V_{GS}=-30V, V_{DS}=0V$

### ON Characteristics

 $T_J = 25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	0.60	0.75	$\Omega$	$V_{GS}=10V, I_D=6.0A$
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
gfs	Forward Transconductance	--	5.2	--	S	$V_{DS}=15V, I_D=6.0A$

### Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$C_{iss}$	Input Capacitance	--	1900	--	$\mu F$	$V_{GS}=0V, V_{DS}=25V, f=1.0MHz$
$C_{rss}$	Reverse Transfer Capacitance	--	33	--		
$C_{oss}$	Output Capacitance	--	150	--		
$Q_g$	Total Gate Charge	--	52	--	$nC$	$V_{DD}=480V, I_D=12A, V_{GS}=0 \text{ to } 10V$
$Q_{gs}$	Gate-to-Source Charge	--	9	--		
$Q_{gd}$	Gate-to-Drain (Miller) Charge	--	20	--		

### Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	25	--	$nS$	$V_{DD}=300V, I_D=12A, V_{GS}=10V, R_g=25\Omega$
$t_{rise}$	Rise Time	--	40	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	150	--		
$t_{fall}$	Fall Time	--	60	--		

**Source-Drain Body Diode Characteristics**  $T_J=25^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
$I_{SD}$	Continuous Source Current <sup>[2]</sup>	--	--	12	A	Integral pn-diode in MOSFET
$I_{SM}$	Pulsed Source Current <sup>[2]</sup>	--	--	48		
$V_{SD}$	Diode Forward Voltage	--	--	1.4	V	$I_S=12\text{A}$ , $V_{GS}=0\text{V}$
$t_{rr}$	Reverse Recovery Time	--	420	--	ns	$V_{GS}=0\text{V}$ $I_F=I_S$ , $di/dt=100\text{A}/\mu\text{s}$
$Q_{rr}$	Reverse Recovery Charge	--	6.0	--	$\mu\text{C}$	

**Note:**[1]  $T_J=+25^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ [2] Pulse width $\leq 380\mu\text{s}$ ; duty cycle $\leq 2\%$ .



## Typical Characteristics

Figure 1. Output Characteristics ( $T_J = 25^\circ\text{C}$ )

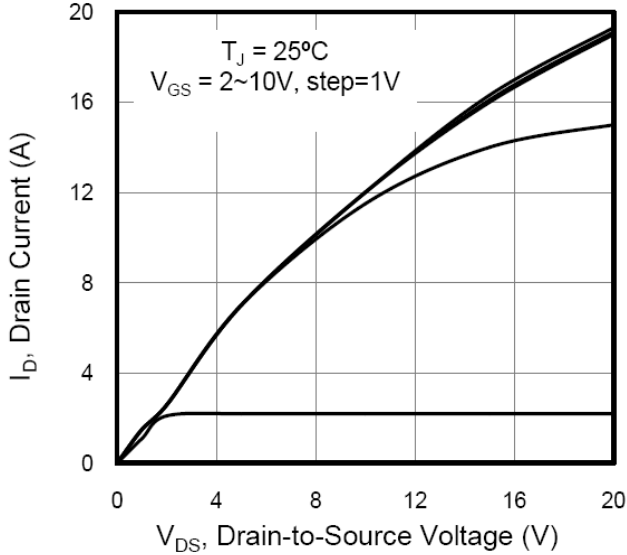


Figure 2. On-Resistance vs. Drain Current

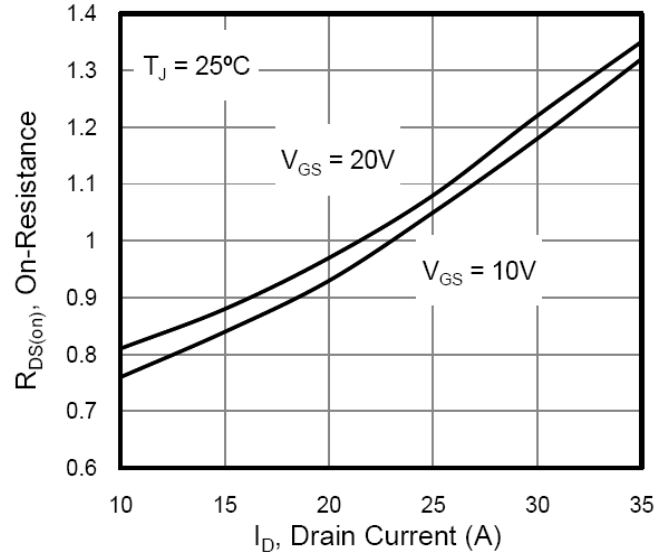


Figure 3.  $BV_{DSS}$  vs. Temperature

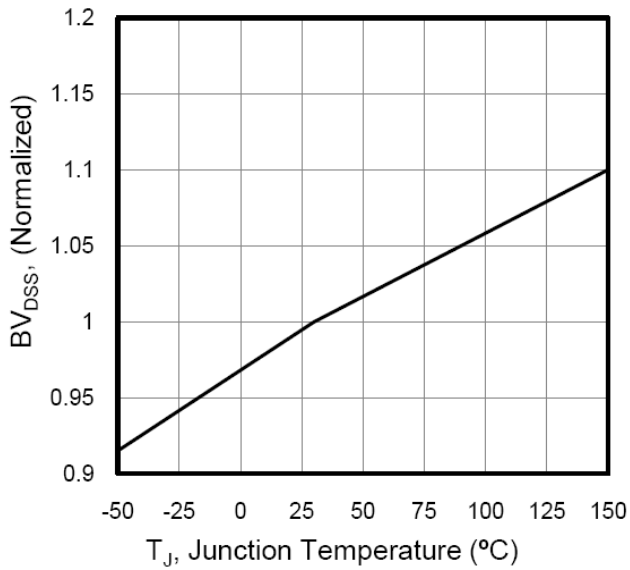


Figure 4. On-Resistance vs. Temperature

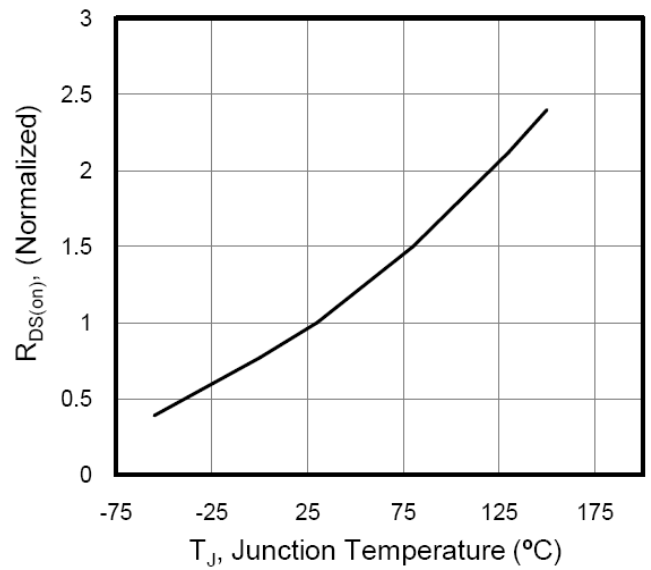




Figure 5. Gate Charge

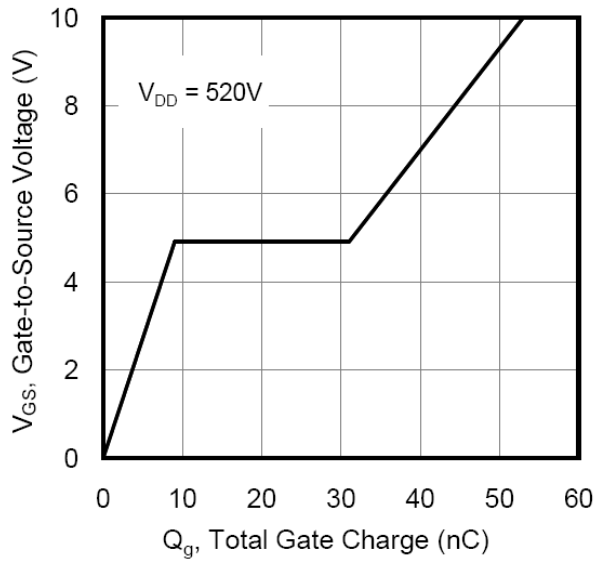


Figure 6. Body Diode Forward Voltage

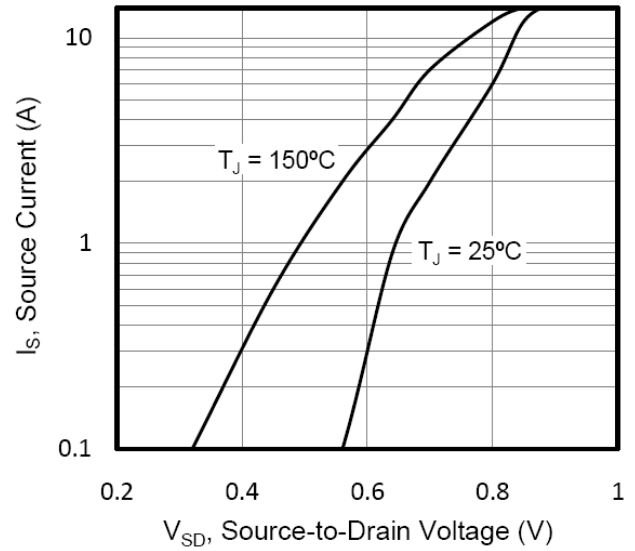


Figure 7. Safe Operating Area

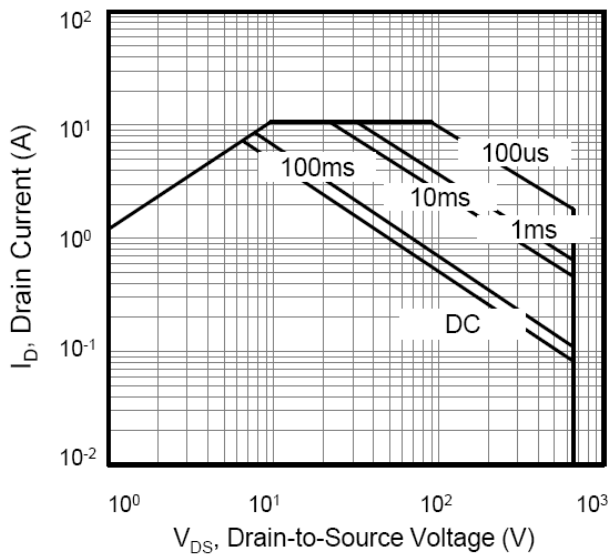
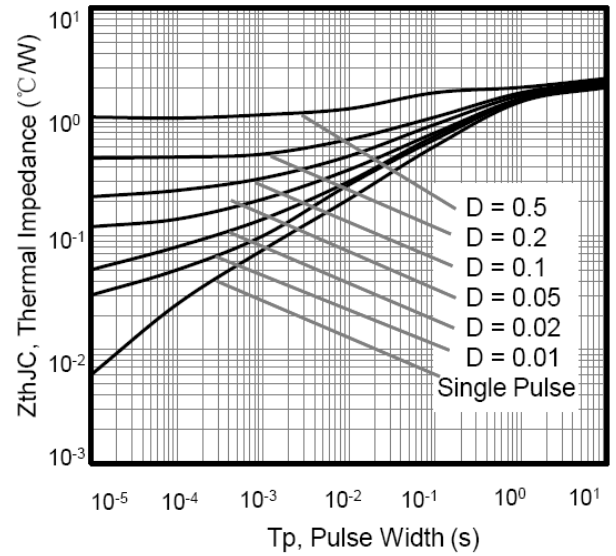


Figure 8. Transient Thermal Impedance





### Test Circuits and Waveforms

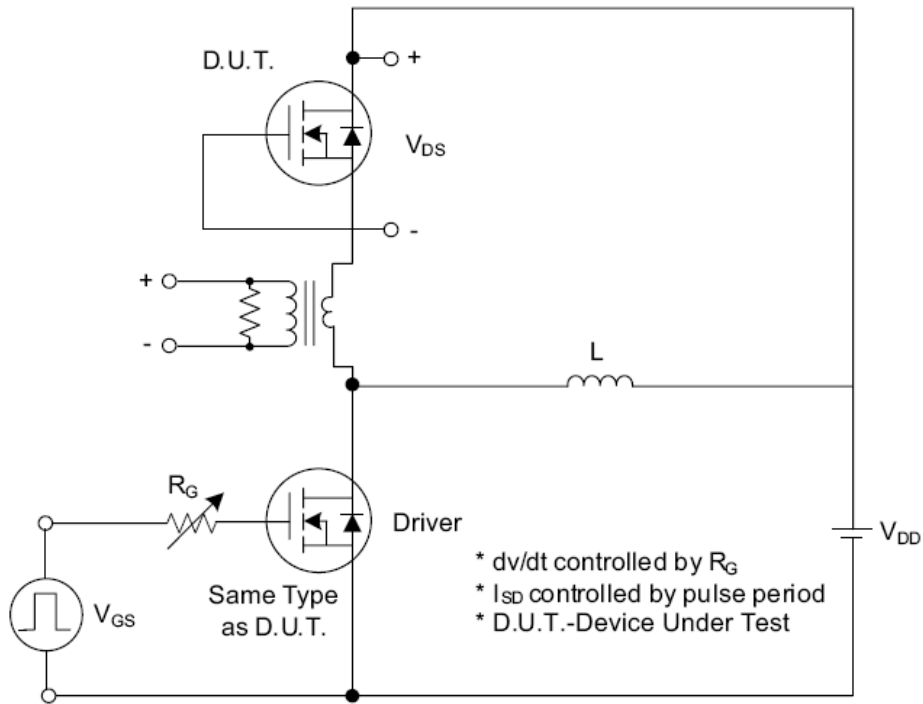


Fig. 1.1 Peak Diode Recovery  $dv/dt$  Test Circuit

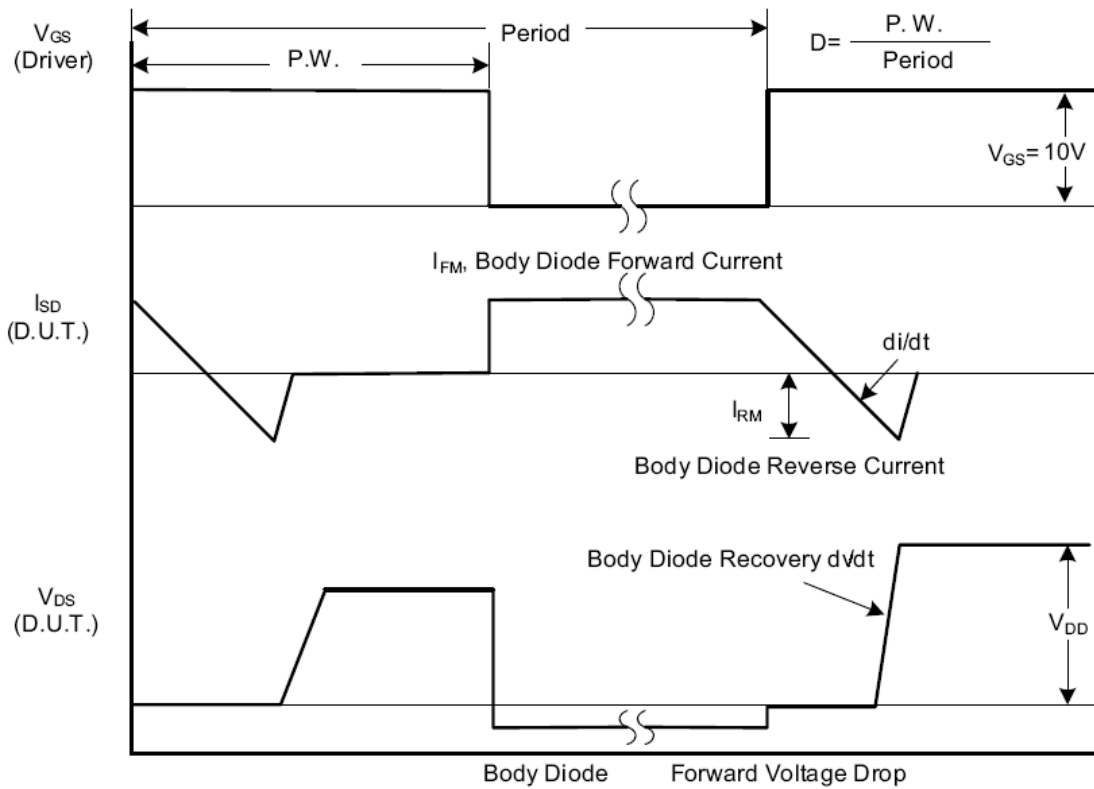


Fig. 1.2 Peak Diode Recovery  $dv/dt$  Waveforms



Test Circuits and Waveforms (Cont.)

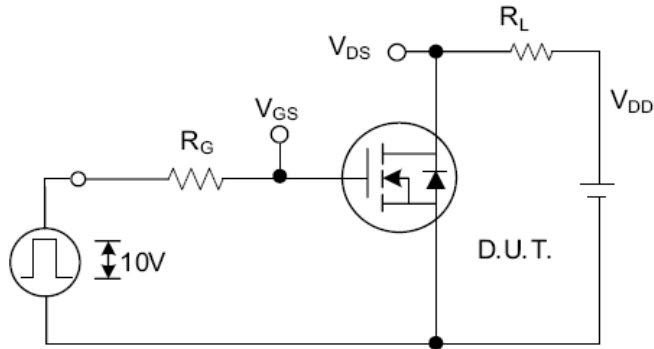


Fig. 2.1 Switching Test Circuit

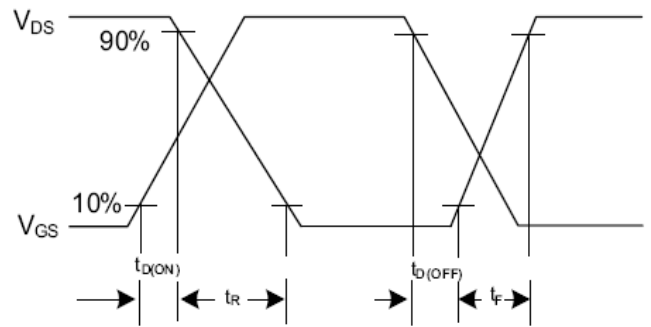


Fig. 2.2 Switching Waveforms

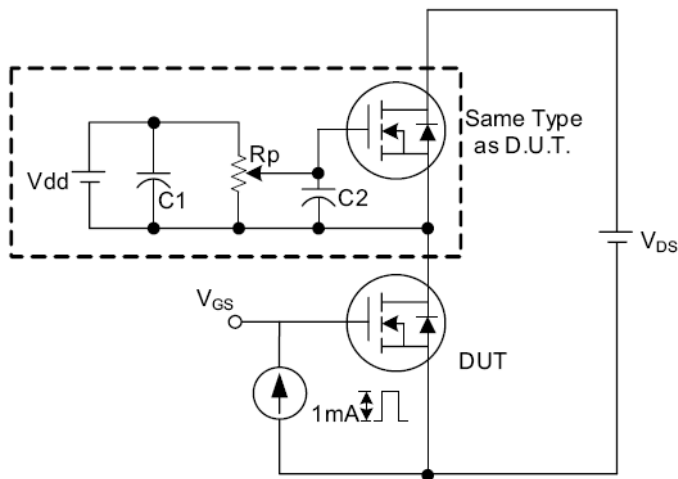


Fig. 3.1 Gate Charge Test Circuit

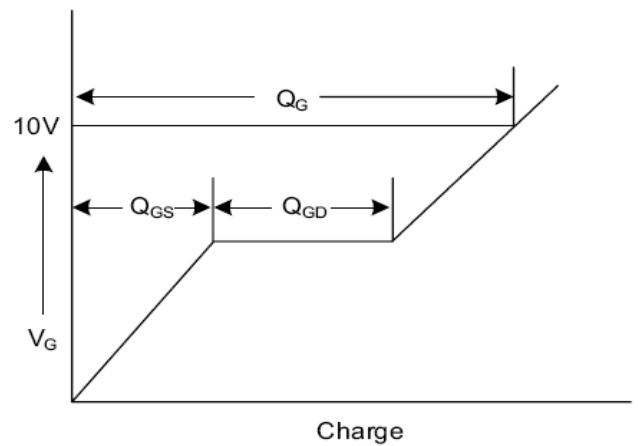


Fig. 3.2 Gate Charge Waveform

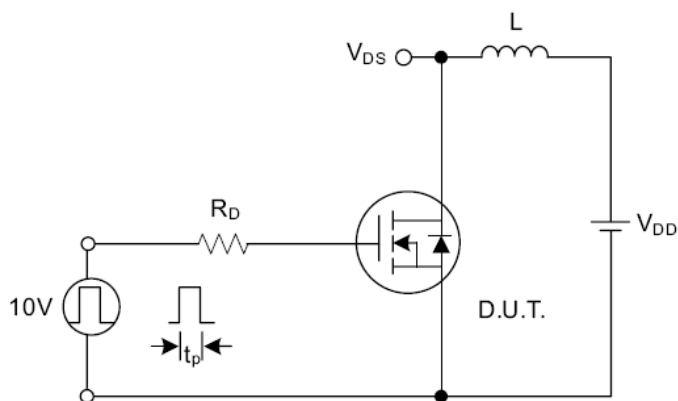


Fig. 4.1 Unclamped Inductive Switching Test Circuit

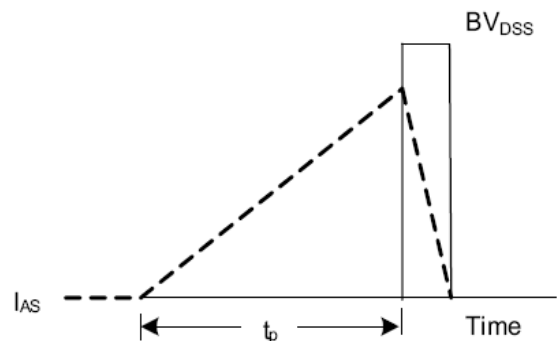


Fig. 4.2 Unclamped Inductive Switching Waveforms