COG128128K

LCD Module User Manual

Rev.	Descriptions	Date
01	Prelimiay Release	2008-09-26

Table of Content

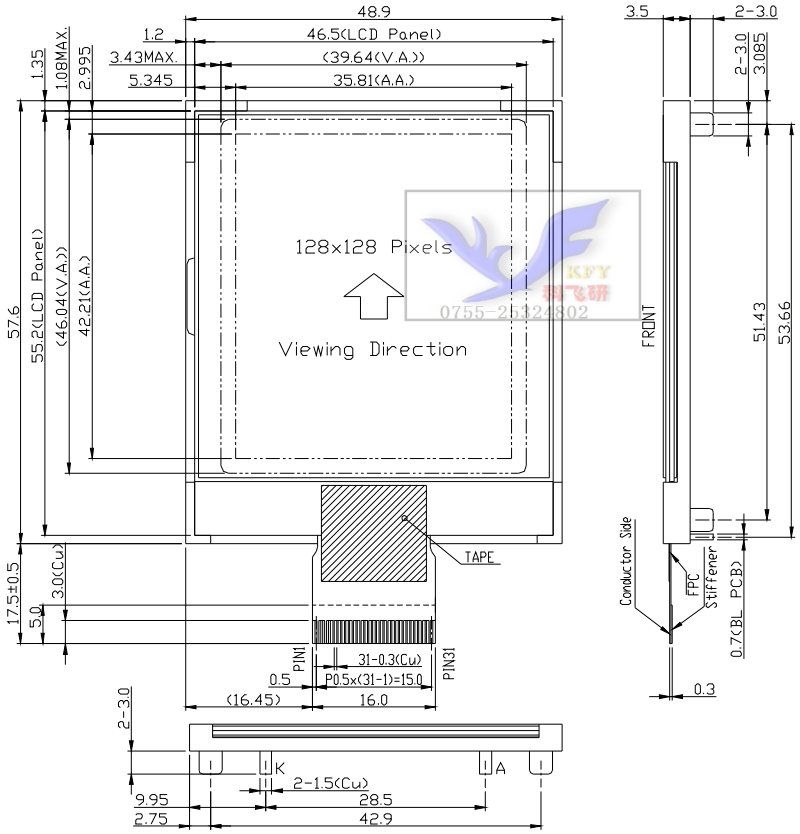
1. Basic Specifications

1.1 Display Specifications

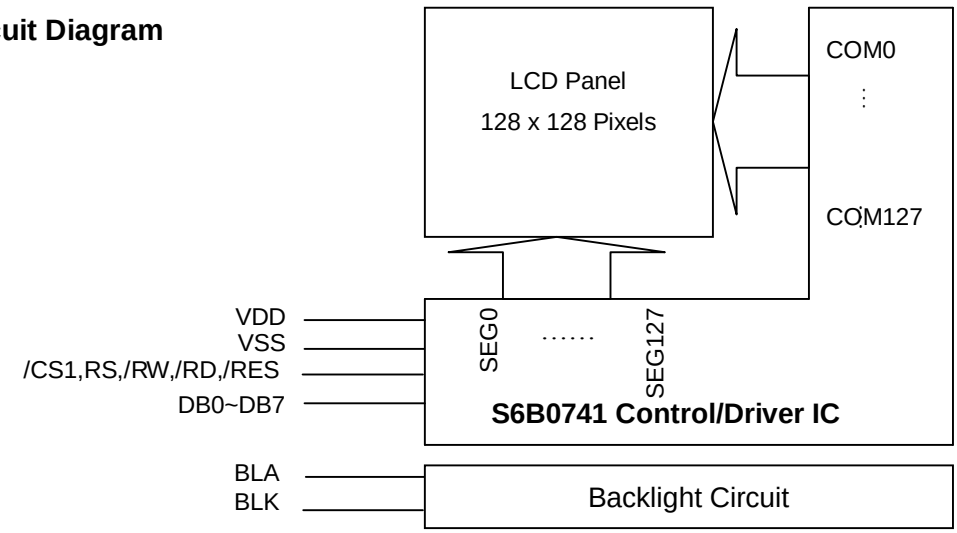
1>LCD Display Mode : FSTN-Gray, Positive, Transmissive
2>Viewing Angle : 6H
3>Driving Method : 1/128 Duty, 1/12 Bias
4>Backlight : Blue

1.2 Mechanical Specifications

1>Outline Dimension : 48.9 x57.6x3.5mm (See attached Outline Drawing for Details)



1.3 Circuit Diagram



1.4 Interface Description

Pin No.	Pin Name	Function
1	PS0	Parallel/Serial Interface Control.
2	PS1	Interface Mode Control.
3	/CSB	Chip selection input
4	/REST	Reset Signal
5	RS	Data/Command control.
6	/WR	Write (W/R) control signal input.
7	/RD	Read (/RD) control signal input.
8~15	DB0~DB7	8-bit Date bus
16	VDD	Power supply voltage (3.3v)
17	VSS	Negative power supply(0V)
18	VOUT	Voltage converter input / output pin
19	CAP5+	Capacitor 5 positive connection pin for voltage converter
20	CAP3+	Capacitor 3 positive connection pin for voltage converter
21	CAP1-	Capacitor 1 negative connection pin for voltage converter
22	CAP1+	Capacitor 1 positive connection pin for voltage converter
23	CAP2+	Capacitor 2 positive connection pin for voltage converter
24	CAP2-	Capacitor 2 negative connection pin for voltage converter
25	CAP4+	Capacitor 4 positive connection pin for voltage converter
26	V4	LCD driver supplay voltage
27	V3	LCD driver supplay voltage
28	V2	LCD driver supplay voltage
29	V1	LCD driver supplay voltage
30	V0	LCD driver supplay voltage
31	OSC1	When using internal clock oscillator, Connect a Resistor between OSC1 and VDD.

2. Absolute Maximum Ratings

Items	Symbol	MIN.	MAX.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	+3.6	V	
	VLCD	-0.3	+15.0	V	
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	-0	+50	℃	
Storage Temperature	Tst	-10	+60	℃	

3. Electrical Characteristics

3.1 DC Characteristics

(V_{SS} = 0V, V_{DD} = 1.8 to 3.3V, Ta = -40 to 85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating Voltage (1)		V_{DD}		1.8	-	3.3	V	V_{DD} (1)
Operating Voltage (2)		V0		4.0	-	15.0	V	V0 (2)
Input Voltage	High	V_{IH}		$0.8V_{DD}$	-	V_{DD}	V	(3)
	Low	V_{IL}		V_{SS}	-	$0.2V_{DD}$		
Output Voltage	High	V_{OH}	I_{OH} = -0.5mA	$0.8V_{DD}$	-	V_{DD}	V	(4)
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	$0.2V_{DD}$		
Input Leakage Current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	(3)
Output Leakage Current		I_{OZ}	VIN = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	(5)
LCD Driver ON Resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn (6)
Operating Frequency		f_{FR}	Ta = 25°C 1/128 Duty, 9 PWM REXT = 620kΩ (*11)	70	85	100	Hz	(7), (11)
Voltage Converter Input Voltage		V_{CI}	× 3	1.8	-	3.6	V	VCI
			× 4	1.8	-	3.6		
			× 5	1.8	-	3.0		
			× 6	1.8	-	2.5		
Voltage Converter Output Voltage		V_{OUT}	x3/×4/×5/×6 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage Regulator Operating Voltage		V_{OUT}		5.4	-	15.0	V	VOUT
Voltage Follower Operating Voltage		V0		4.0	-	15.0	V	V0 (8)
Reference Voltage		V_{REF}	Ta = 25°C	2.04	2.10	2.16	V	(9)

(V_{DD} = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic Current Consumption	I_{DD}	V0 - V_{SS} = 12.0V, x5 boosting, duty = 1/128, normal mode (Display Off)	-	100	150	µA	(10)
		V0 - V_{SS} = 12.0V, x5 boosting, duty = 1/128, normal mode (Display On , Checker Pattern)	-	200	300	µA	(10)

(V_{DD} = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep Mode Current	I_{DDS1}	During Sleep	-	-	2	µA	(10)

Duty ratio	Item	f_{CL}	f_{OSC}
1/N	On-chip oscillator circuit is used	f_{FR} x N	f_{FR} x PWM x 2 x N

(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: frame frequency, N = 16 to 129)

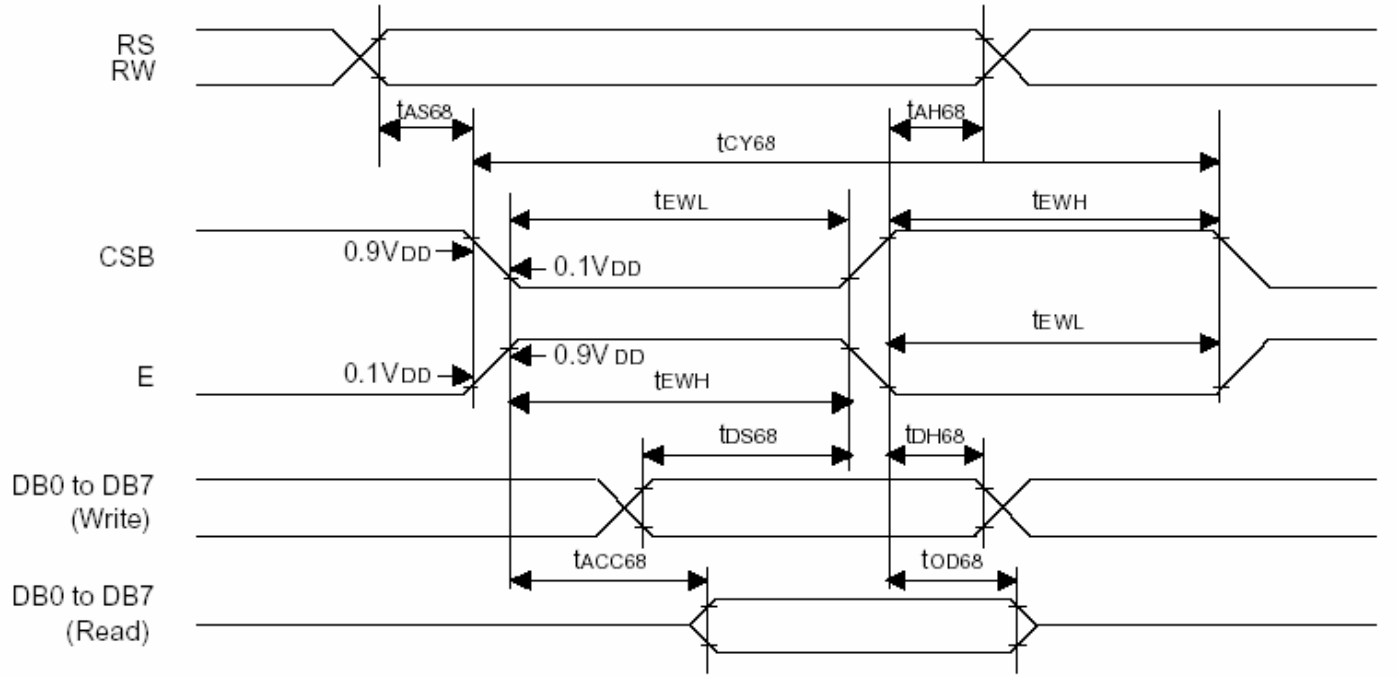
3.2 LED Backlight Circuit

Vss = 0V,Top = 25℃

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Forword Voltage	Vf BLA	-	2.0	3.5	V	2.0V
Forword Current	If BLA	15	20	30	mA	2.0V

3.3 AC Characteristic

3.3.1 6800 Mode System Bus Tim



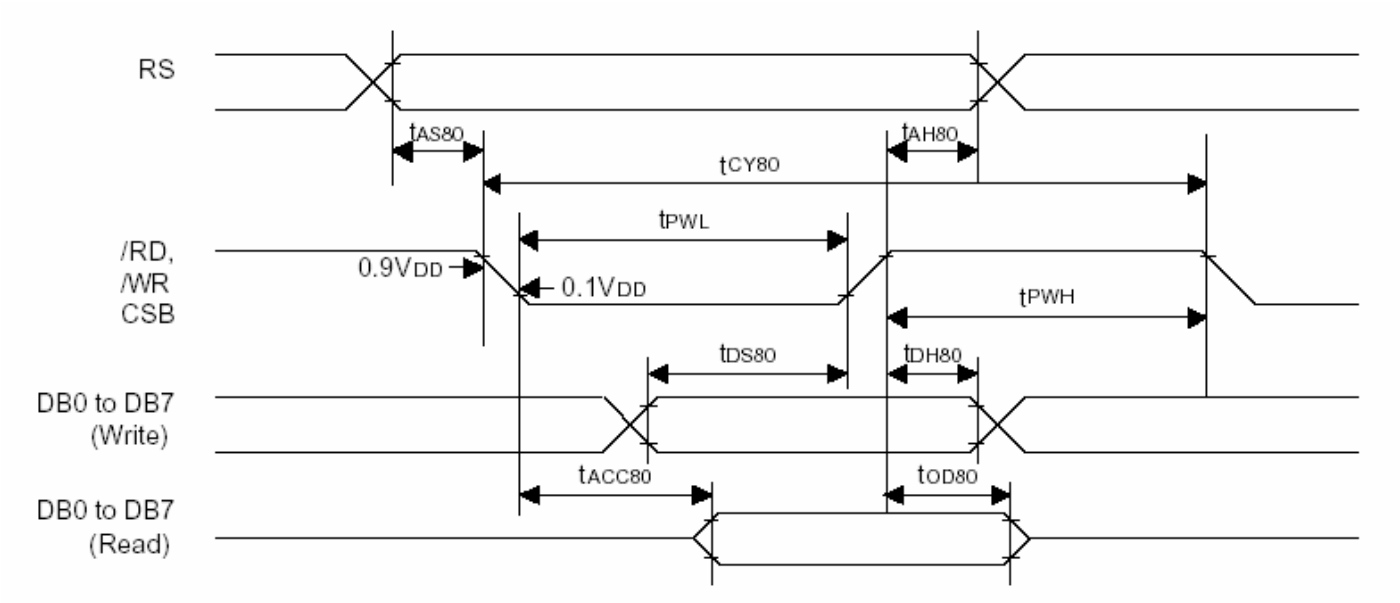
(V_{DD} = 1.8V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address Setup Time Address Hold Time	RS RW_WR	t_{AS68} t_{AH68}		0 0	- -	ns
System Cycle Time For Write System Cycle Time For Read		t_{CY68} t_{CY68}		150 330	-	ns
Enable Width High Enable Width Low	E_RD (E)	t_{EWH} t_{EWL}		60 60	- -	ns
Data Setup Time Data Hold Time	DB0 to DB7	t_{DS68} t_{DH68}		40 10	- -	ns
Read Access Time Output Disable Time		t_{ACC68} t_{OD68}	C_L = 100 pF	15 10	- 50	ns

(V_{DD} = 2.7V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address Setup Time Address Hold Time	RS RW_WR	t_{AS68} t_{AH68}		0 0	- -	ns
System Cycle Time For Write System Cycle Time For Read		t_{CY68} t_{CY68}		100 166	-	ns
Enable Width High Enable Width Low	E_RD (E)	t_{EWH} t_{EWL}		40 40	- -	ns
Data Setup Time Data Hold Time	DB0- DB7	t_{DS68} t_{DH68}		30 5	- -	ns
Read Access Time Output Disable Time		t_{ACC68} t_{OD68}	C_L = 100 pF	15 10	- 50	ns

3.3.2 8080 Mode System Bus Tim



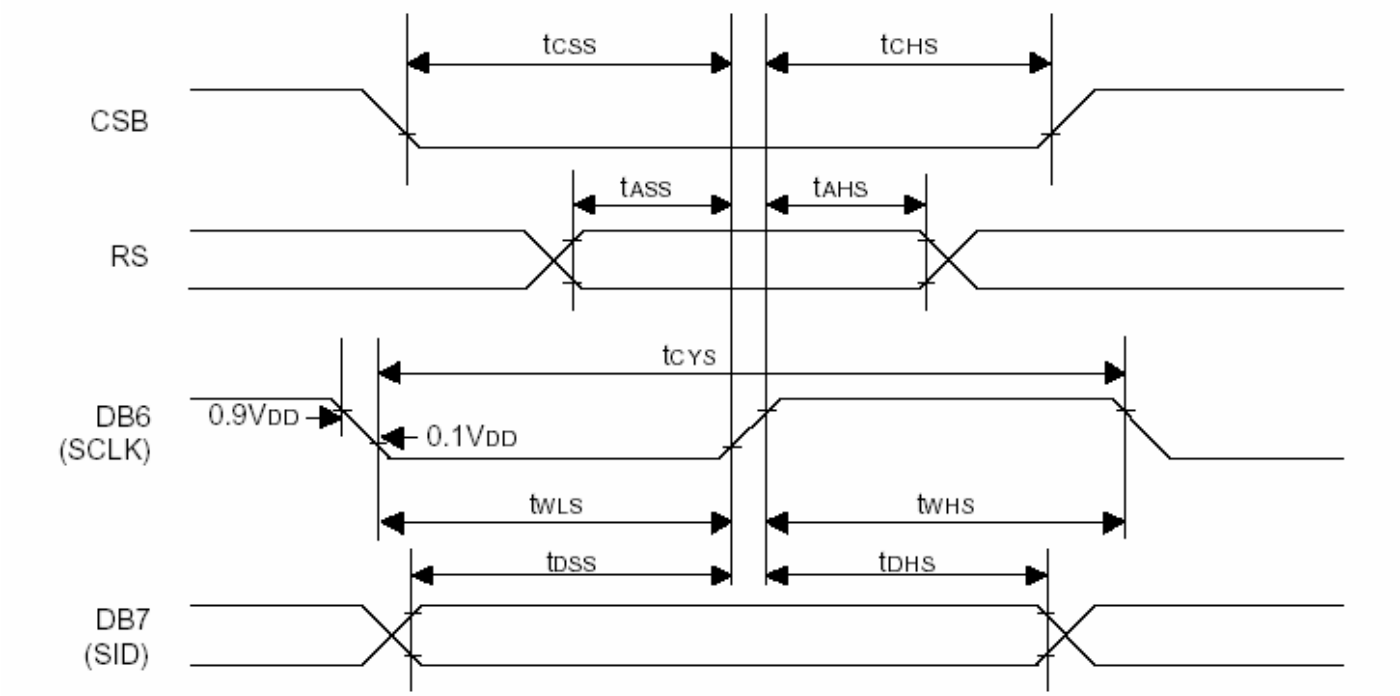
(V_{DD} = 1.8V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address Setup Time Address Hold Time	RS	t_{AS80} t_{AH80}		0 0	- -	ns
System Cycle Time For Write System Cycle Time For Read		t_{CY80} t_{CY80}		150 330	-	ns
Pulse Width Low Pulse Width High	/WR /RD	t_{PWL} t_{PWH}		60 60	- -	ns
Data Setup Time Data Hold Time	DB0-DB7	t_{DS80} t_{DH80}		40 10	- -	ns
Read Access Time Output Disable Time		t_{ACC80} t_{OD80}	CL = 100 pF	15 10	- 50	ns

(V_{DD} = 2.7V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address Setup Time Address Hold Time	RS	t_{AS80} t_{AH80}		0 0	- -	ns
System Cycle Time For Write System Cycle Time For Read		t_{CY80} t_{CY80}		100 166	-	ns
Pulse Width Low Pulse Width High	/WR /RD	t_{PWL} t_{PWH}		40 40	- -	ns
Data Setup Time Data Hold Time	DB0-DB7	t_{DS80} t_{DH80}		30 5	- -	ns
Read Access Time Output Disable Time		t_{ACC80} t_{OD80}	CL = 100 pF	15 10	- 50	ns

3.3.3 Seiral Interface



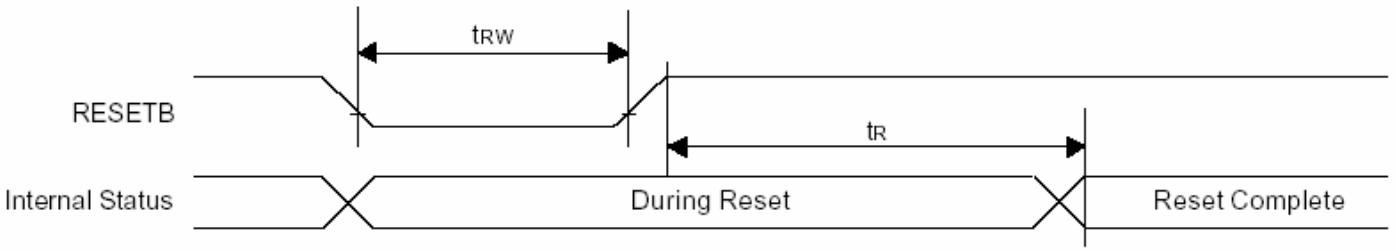
(V_{DD} = 1.8V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial Clock Cycle SCLK High Pulse Width SCLK Low Pulse Width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}		111 60 60	- - -	ns
Address Setup Time Address Hold Time	RS	t_{ASS} t_{AHS}		60 60	- -	ns
Data Setup Time Data Hold Time	DB7 (SID)	t_{DSS} t_{DHS}		60 60	- -	ns
CSB Setup Time CSB Hold Time	CSB	t_{CSS} t_{CHS}		60 1/2 * tCYS	- -	ns

(V_{DD} = 2.7V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial Clock Cycle SCLK High Pulse Width SCLK Low Pulse Width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}		58.8 30 30	- - -	ns
Address Setup Time Address Hold Time	RS	t_{ASS} t_{AHS}		30 30	- -	ns
Data Setup Time Data Hold Time	DB7 (SID)	t_{DSS} t_{DHS}		30 30	- -	ns
CSB Setup Time CSB Hold Time	CSB	t_{CSS} t_{CHS}		30 1/2 * tCYS	- -	ns

3.4 Reset Timing



(V_{DD} = 1.8 to 3.3V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset Low Pulse Width	RESETB	t_{RW}		1000	-	ns
Reset Time	-	t_R		-	1000	ns

4. Function specifications

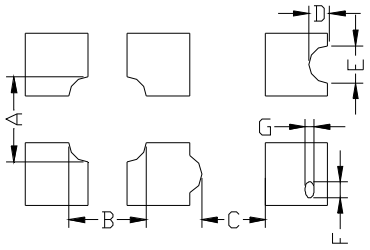
4.1 The Parallel Interface

4.2 Basic Operating Sequence

Initialization Sequence

	A0	D7	D6	D5	D4	D3	D2	D1	D0	hex	Note
Turn on Power Supply VDD & VSS While maintaining /RES at LOW	-	-	-	-	-	-	-	-	-	-	-
Wait until power supply is stabilized	-	-	-	-	-	-	-	-	-	-	-
Release the /RES Reset Signal (/RES = High)	-	-	-	-	-	-	-	-	-	-	
LCD Bias = 1/12	0	0	1	0	1	0	1	1	1	57H	
ADC = Normal	0	1	0	1	0	0	0	0	1	A1H	No flip on x-direction (SEG)
SHL = Reverse	0	1	1	0	0	1	0	0	0	C8H	Flip on y- direction (COM)
Oscillator on start	0	1	0	1	0	1	0	0	0	A8H	
Initial Display Line = 0	0	0	1	0	0	0	0	0	0	44H	Display RAM “Page 0-D0” Matched to top line of the LCD
	0	0	0	0	0	0	0	0	0	00H	Start From Com0
Power Control Voltage Follower = OFF Voltage Regulator = OFF Voltage Converter = ON	0	0	0	1	0	1	1	0	0	2CH	Turn on the internal Voltage Converter and wait until VOUT stable
Delay 50ms	-	-	-	-	-	-	-	-	-	-	
Power Control Voltage Follower = OFF Voltage Regulator = ON Voltage Converter = ON	0	0	0	1	0	1	1	1	0	2EH	Turn on the internal Voltage Regulator and wait until VOUT stable
Delay 50ms	-	-	-	-	-	-	-	-	-	-	
Power Control Voltage Follower = ON Voltage Regulator = ON Voltage Converter = ON	0	0	0	1	0	1	1	1	1	2FH	Turn on the internal Voltage Follower and wait until VOUT stable
Delay 50ms	-	-	-	-	-	-	-	-	-	-	
Boost Set	0	0	1	1	0	0	1	1	1		5 times boosting
Regulator Resistor Select	0	0	0	1	0	0	1	0	1	25H	Set the built-in resistor ratio to middle
Set Reference Voltage Mode	0	1	0	0	0	0	0	0	1	81H	Set to the middle of the range it may be adjused For achieving the best display contrast
Set Reference Voltage Resistor	0	0	0	1	0	0	0	0	0	25H	
Set FRC and PWM mode	0	1	0	0	1	0	0	1	1	93H	
Set Page Address = 0	0	1	0	1	1	0	0	0	0	B0H	Specify the display data RAM page address to 00H
Set Column Address (Upper -4bit = 0)	0	0	0	0	1	0	0	0	0	10H	Specify the display data RAM column address to 00H
Set Column Address (Lower-4bit =4)	0	0	0	0	0	0	1	0	0	00H	
Write Display Data	1	Display Data									-

5. Inspection Standards

Item	Criterion for defects	Defect type
1) Display on inspection	(1) Non display (2) Vertical line is deficient (3) Horizontal line is deficient (4) Cross line is deficient	Major
2) Black / White spot	Size Φ(mm) Acceptable number Φ≤0.3 Ignore (note) 0.3<Φ≤0.45 3 0.45<Φ≤0.6 1 0.6<Φ 0	Minor
3) Black / White line	Length (mm) Width (mm) Acceptable number L≤10 W≤0.03 Ignore 5.0≤L≤10 0.03<W≤0.04 3 5.0≤L≤10 0.04<W≤0.05 2 1.0≤L≤10 0.05<W≤0.06 2 1.0≤L≤10 0.06<W≤0.08 1 L≤10 0.08<W follows 2) point defect Defects separate with each other at an interval of more than 20mm	Minor
4) Display pattern	 $\frac{A+B}{2}\leq 0.28$ 0<C $\frac{D+E}{2}\leq 0.25$ $\frac{F+G}{2}\leq 0.25$ Note: 1) Up to 3 damages acceptable 2) Not allowed if there are two or more pinholes every three-fourth inch.	Minor
5) Spot-like contrast irregularity	Size Φ(mm) Acceptable Number Φ≤0.7 Ignore (note) 0.7<Φ≤1.0 3 1.0<Φ≤1.5 1 1.5<Φ 0 Note: 1) Conformed to limit samples. 2) Intervals of defects are more than 30mm.	Minor
6) Bubbles in polarizer	Size Φ(mm) Acceptable Number Φ≤0.4 Ignore (note) 0.4<Φ≤0.65 2 0.65<Φ≤1.2 1 1.2<Φ 0	Minor
7) Scratches and dent on the polarizer	Scratches and dent on the polarizer shall be in the accordance with “2) Black/white spot”, and “3) Black/White line”.	Minor
8) Stains on the surface of LCD panel	Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning.	Minor
9) Rainbow color	No rainbow color is allowed in the optimum contrast on state within the active area.	Minor
10) Viewing area encroachment	Polarizer edge or line is visible in the opening viewing area due to polarizer shortness or sealing line.	Minor
11) Bezel appearance	Rust and deep damages that are visible in the bezel are rejected.	Minor
12) Defect of land surface contact	Evident crevices that are visible are rejected.	Minor
13) Parts mounting	(1) Failure to mount parts (2) Parts not in the specifications are mounted (3) For example: Polarity is reversed, HSC or TCP falls off.	Minor
14) Part alignment	(1) LSI, IC lead width is more than 50% beyond pad outline. (2) More than 50% of LSI, IC leads is off the pad outline.	Minor
15) Conductive foreign matter (solder ball, solder hips)	(1) 0.45<Φ, N≥1 (2) 0.3<Φ≤0.45, N≥1, Φ: Average diameter of solder ball (unit: mm) (3) 0.5<L, N≥1, L: Average length of solder chip (unit: mm)	Minor
16) Bezel flaw	Bezel claw missing or not bent	Minor
17) Indication on name plate (sampling indication label)	(1) Failure to stamp or label error, or not legible.(all acceptable if legible) (2) The separation is more than 1/3 for indication discoloration, in which the characters can be checked.	Minor

6. Handling Precautions

6.1 Mounting method

A panel of LCD module made by our company consists of two thin glass plates with polarizers that easily get damaged.
And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board (PCB), extreme care should be used when handling the LCD modules.

6.2 Cautions of LCD handling and cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.
-Isopropyl alcohol
-Ethyl alcohol
-Trichlorotriflorothane
Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.
Do not use the following solvent:
-Water
-Ketene
-Aromatics

6.3 Caution against static charge

The LCD module use C-MOS LSI drivers. So we recommend you:
Connect any unused input terminal to V_{dd} or V_{ss}. Do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

6.4 Packaging

-Module employs LCD elements, and must be treated as such. Avoid intense shock and falls from a height.
-To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

6.5 Caution for operation

-It is an indispensable condition to drive LCD module within the limits of the specified voltage since the higher voltage over the limits may cause the shorter life of LCD module.
-An electrochemical reaction due to DC (direct current) causes LCD undesirable deterioration so that the uses of DC (direct current) drive should be avoided.
-Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD module may show dark color in them. However those phenomena do not mean malfunction or out of order of LCD module, which will come back in the specified operating temperature.

6.6 Storage

In the case of storing for a long period of time, the following ways are recommended:
-Storage in polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with not desiccant.
-Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping the storage temperature range.
-Storing with no touch on polarizer surface by any thing else.

6.7 Safety

-It is recommendable to crash damaged or unnecessary LCD into pieces and to wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
-When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well at once with soap and water.