S6B0741

128 SEG / 129 COM DRIVER & CONTROLLER FOR 4 GRAY SCALE STN LCD

March. 2001

Ver. 2.2

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.

2. Always test and inspect products under the environment with no penetration of light.

S6B0741 Specification Revision History		
Version	**Content**	**Date**
0.0	Preliminary specification (short form)	June 8, 1999
0.1	Preliminary specification (full set)	July 14, 1999
0.2	Added temporary pin number (page 5,6)	July 15, 1999
0.3	Removed HPMB, CS2 pins CS1B pin → CSB pin V_{OL} Max.: 0.3V_{DD} → 0.2V_{DD} , V_{OH} Min.: 0.7V_{DD} → 0.8V_{DD} (page 59)	July 30, 1999
0.4	Removed CLS, OSCCK, OSC2 pins (page 7,8) Read internal status: MF, DS ID is added, ADC is removed (Page 35, 39) RESET flag: 0: display ON, 1: display OFF → 0: display OFF, 1: display ON (Page 39)	Aug. 12, 1999
0.5	Changed input pin order, add RESETB pin (page 5) Added VR, VEXT pin connection (page 8) VR: When using internal resistors (INTRS = "H"), open this pin VEXT: When using internal voltage regulator, connect to VDD, VSS or open this pin Added test pin connection (page 9) TEST1,TEST2: connect to " VDD" TEST3,TEST4,TEST5: connect to " VSS" Changed OSC resistance connection (page8, 23) Between OSC1 and OSC2 → between OSC1 and VDD	Aug. 30, 1999
0.6	Removed TEST2, TEST3, TEST4, TEST5, TEST6, TEST7 pins Added COMS, COMS1 for ICON display. Added ICON control register ON/OFF instruction.	Sep. 30, 1999
0.7	Removed COMS, COMS1 for ICON display. Removed ICON control register ON/OFF instruction.	Oct. 4, 1999
1.0	Added COMS, COMS1 for ICON display. Added ICON control register ON/OFF instruction. Modified bit settings for partial display command. Relaxed V_{IH} and V_{IL} specifications. Modified interface timing specs.	Jan. 18, 2000
1.1	Added 6800-mode interface description for data latch with CSB (page 14) C2 CAP value : 0.1 to 0.47uF → 0.47 to 2.0uF (page 34) Added Icon Mode Disabled to the Reset default list. (page 36) Added description of the column address operation. (page 40) Added that Display On/Off command has priority over Entire Display On/Off and Reverse Display On/Off. (page 44) Added N-line inversion command description (page 47) The lower limit of VOUT, V0 - V4 : +0.3V → -0.3V (page 60)	Jan. 24, 2000
1.2	The upper limit of V1 - V4 : V0 → V0 + 0.3V (page 60)	Feb. 8, 2000

S6B0741 Specification Revision History (Continued)		
Version	**Content**	**Date**
2.0	Changed temperature coefficient value (page 1) Determined current consumption (page 2, 62) Added remarks about oscillator resistor (page 61, 63) Changed parallel interface timing (page 17, 64, 65)	Jun. 26, 2000
2.1	Removed wrong description about display data ram. (page 1)	Aug. 6, 2000
2.2	Added detail information for several items	Feb.2001
2.3	Determined maximum operating oscillator frequency (page 63, 65)	Jan.2002

CONTENTS

INTRODUCTION

The S6B0741 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. It contains 128 segment and 129 common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit parallel display data and stores in an on-chip display data RAM of 128 x 129 x 2 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

4-level (White, Light Gray, Dark Gray, Black) Gray Scale Display with PWM and FRC Methods

DDRAM data [2n: 2n+1]	00	01	10	11
Gray scale	White	Light gray	Dark gray	Dark

(Accessible column address, n = 0, 1, 2, ……, 125, 126, 127)

Driver Output Circuits
— 128 segment outputs/129 common outputs

Applicable Duty Ratios

Duty Ratio	Applicable LCD Bias	Maximum Display Area
1/16 - 1/128 (ICON disabled) 1/17 - 1/129 (ICON enabled)	1/5 to 1/12	129 × 128

— Various partial display
— Partial window moving & data scrolling

On-chip Display Data RAM
— Capacity: 129 × 128 × 2 = 33,024bits

Microprocessor Interface
— 8-bit parallel bi-directional interface with 6800-series or 8080-series
— SPI (serial peripheral interface) available (only write operation)

On-chip Low Power Analog Circuit
— On-chip oscillator circuit
— Voltage converter (x3, x4, ×5 or x6)
— Voltage regulator (temperature coefficient: -0.125%/°C, or external input)
— On-chip electronic contrast control function (64 steps)
— Voltage follower (LCD bias : 1/5 to 1/12)

Operating Voltage Range
— Supply voltage (V_{DD}): 1.8 to 3.3V
— LCD driving voltage (V_{LCD} = V0 - V_{SS}): 4.0 to 15.0 V

Low Power Consumption
— 300 μA Max. (operation)
— 2 μA Max. (sleep mode)

Package Type
— Slim chip for TCP

BLOCK DIAGRAM

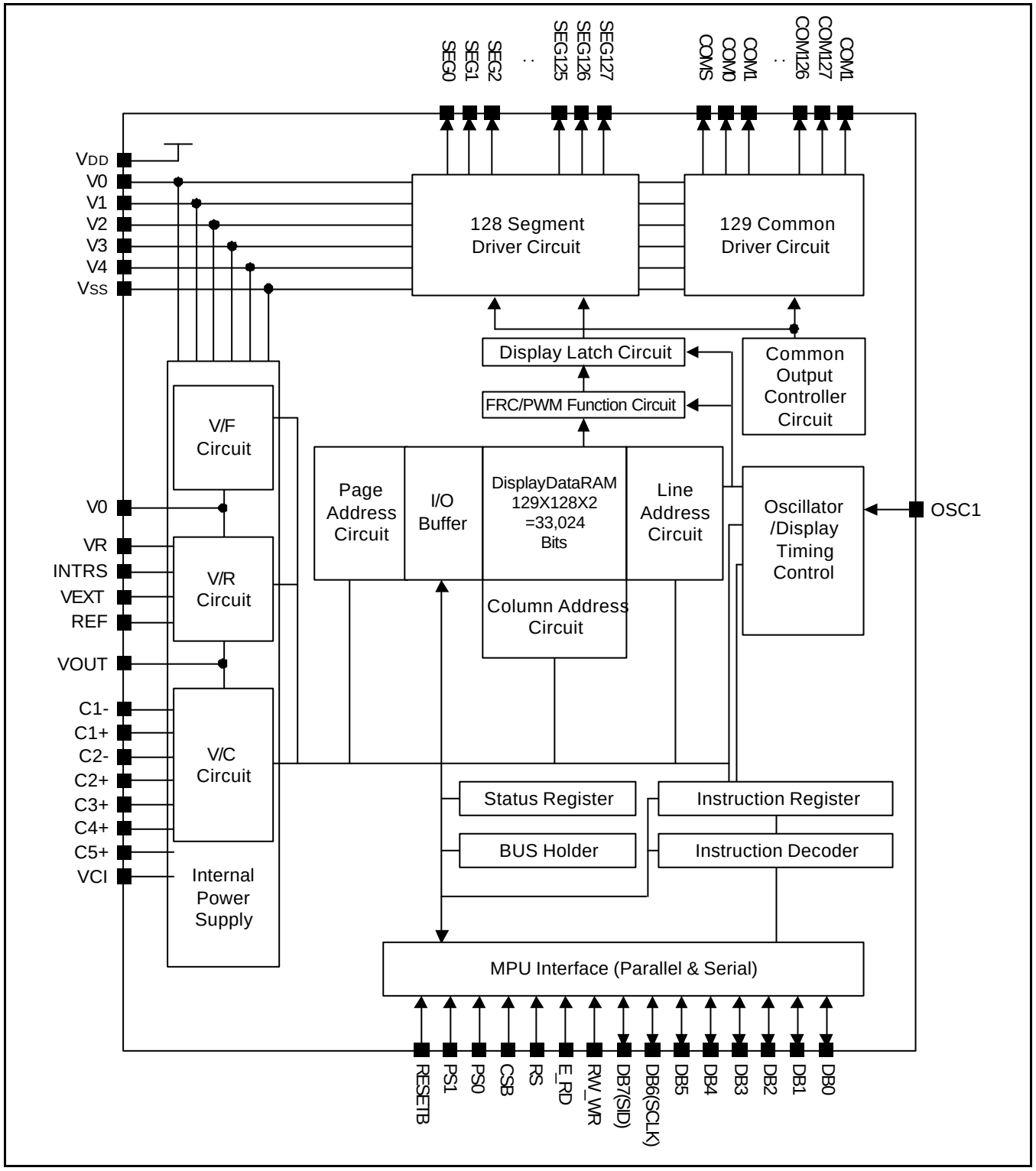


Figure 1. Block Diagram

PAD CONFIGURATION

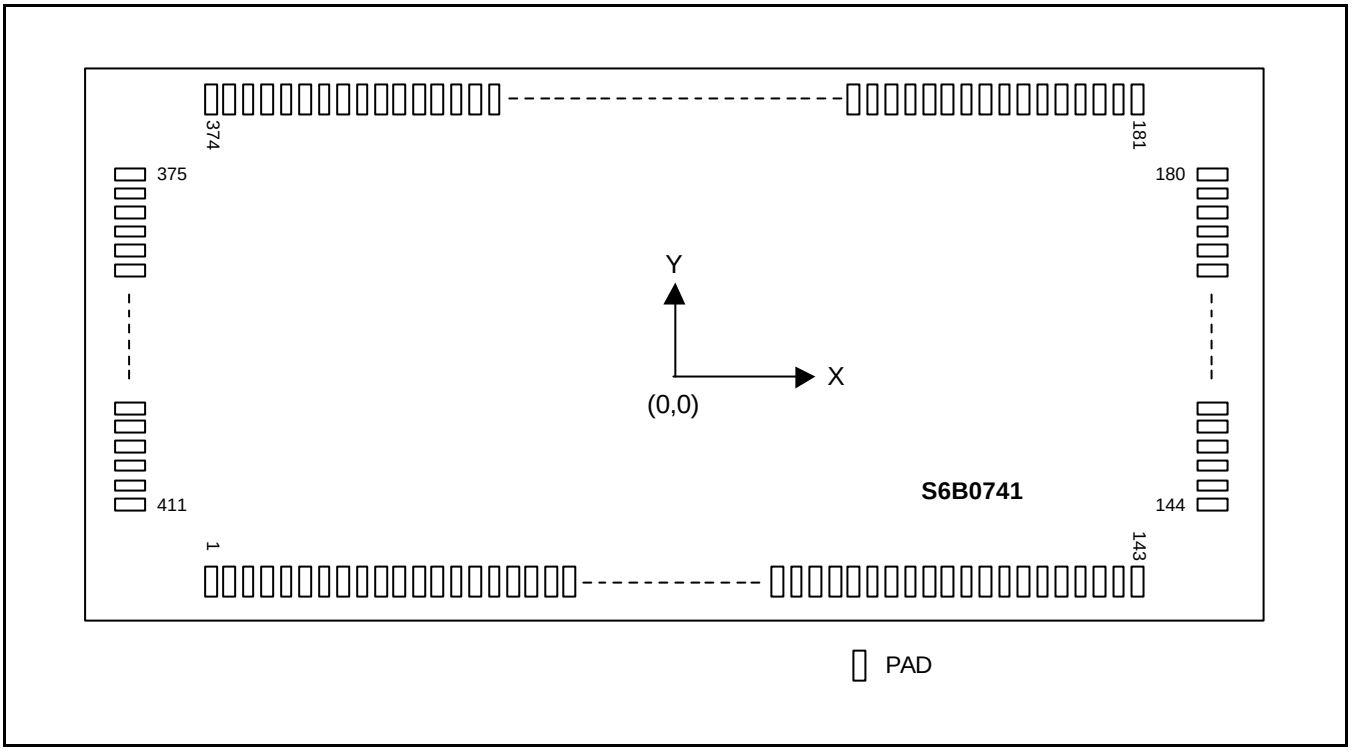
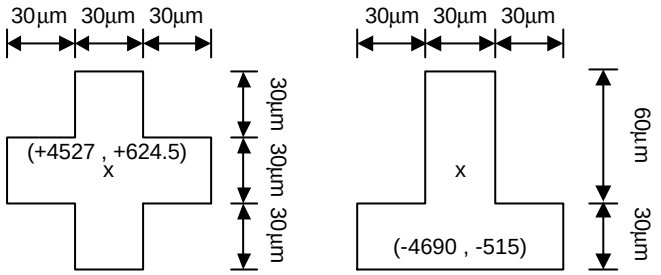


Figure 2. S6B0741 Chip Configuration

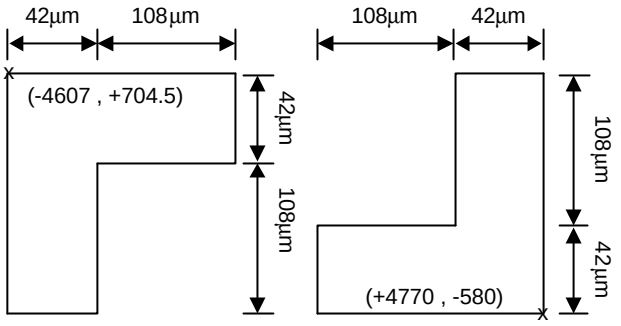
Table 1. S6B0741 Pad Dimensions

Items	Pad No.	Size		Unit
		X	Y	
Chip size	-	10580	2520	μm
Pad pitch	1-143	70		
	144-178, 183-372, 377-411	52		
	179-182, 373-376	80		
Bumped pad size	1-143	42	92	
	145 -178, 377-410	70	34	
	183-372	34	70	
	144, 179-180, 375-376, 411	70	62	
	181-182, 373-374	62	70	
Bumped pad height	ALL PAD	14(Typ.)		

COG Align Key Coordinate



ILB Align Key Coordinate(with Gold Bump*)



* When designing electrode pattern must be prohibited on this area (ILB Align Key). If electrode pattern is used for routing over this area, it can be happened pattern-short through bumped pattern on ILB Align Key.

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y
1	DUMMY	-4970	-1145	35	DUMMY	-2590	-1145	69	RS	-210	-1145
2	DUMMY	-4900	-1145	36	DUMMY	-2520	-1145	70	RW_WR	-140	-1145
3	DUMMY	-4830	-1145	37	DUMMY	-2450	-1145	71	VSS	-70	-1145
4	DUMMY	-4760	-1145	38	DUMMY	-2380	-1145	72	E_RD	0	-1145
5	DUMMY	-4690	-1145	39	DUMMY	-2310	-1145	73	VDD	70	-1145
6	DUMMY	-4620	-1145	40	DUMMY	-2240	-1145	74	DB0	140	-1145
7	DUMMY	-4550	-1145	41	DUMMY	-2170	-1145	75	DB1	210	-1145
8	DUMMY	-4480	-1145	42	DUMMY	-2100	-1145	76	DB2	280	-1145
9	DUMMY	-4410	-1145	43	DUMMY	-2030	-1145	77	DB3	350	-1145
10	DUMMY	-4340	-1145	44	DUMMY	-1960	-1145	78	DB4	420	-1145
11	DUMMY	-4270	-1145	45	DUMMY	-1890	-1145	79	DB5	490	-1145
12	DUMMY	-4200	-1145	46	DUMMY	-1820	-1145	80	DB6	560	-1145
13	DUMMY	-4130	-1145	47	DUMMY	-1750	-1145	81	DB7	630	-1145
14	DUMMY	-4060	-1145	48	DUMMY	-1680	-1145	82	VDD	700	-1145
15	DUMMY	-3990	-1145	49	DUMMY	-1610	-1145	83	VDD	770	-1145
16	DUMMY	-3920	-1145	50	DUMMY	-1540	-1145	84	VDD	840	-1145
17	DUMMY	-3850	-1145	51	DUMMY	-1470	-1145	85	VDD	910	-1145
18	DUMMY	-3780	-1145	52	DUMMY	-1400	-1145	86	VDD	980	-1145
19	DUMMY	-3710	-1145	53	DUMMY	-1330	-1145	87	VDD	1050	-1145
20	DUMMY	-3640	-1145	54	DUMMY	-1260	-1145	88	VCI	1120	-1145
21	DUMMY	-3570	-1145	55	DUMMY	-1190	-1145	89	VSS	1190	-1145
22	DUMMY	-3500	-1145	56	DUMMY	-1120	-1145	90	VSS	1260	-1145
23	DUMMY	-3430	-1145	57	DUMMY	-1050	-1145	91	VSS	1330	-1145
24	DUMMY	-3360	-1145	58	DUMMY	-980	-1145	92	VSS	1400	-1145
25	DUMMY	-3290	-1145	59	VDD	-910	-1145	93	VSS	1470	-1145
26	DUMMY	-3220	-1145	60	TEST1	-840	-1145	94	VSS	1540	-1145
27	DUMMY	-3150	-1145	61	VSS	-770	-1145	95	VSS	1610	-1145
28	DUMMY	-3080	-1145	62	PS0	-700	-1145	96	VSS	1680	-1145
29	DUMMY	-3010	-1145	63	VDD	-630	-1145	97	VOUT	1750	-1145
30	DUMMY	-2940	-1145	64	PS1	-560	-1145	98	VOUT	1820	-1145
31	DUMMY	-2870	-1145	65	VSS	-490	-1145	99	V5+	1890	-1145
32	DUMMY	-2800	-1145	66	CSB	-420	-1145	100	V5+	1960	-1145
33	DUMMY	-2730	-1145	67	RESETB	-350	-1145	101	V3+	2030	-1145
34	DUMMY	-2660	-1145	68	VDD	-280	-1145	102	V3+	2100	-1145

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y
103	C1-	2170	-1145	140	DUMMY	4760	-1145	177	COM31	5166	766
104	C1-	2240	-1145	141	DUMMY	4830	-1145	178	COM30	5166	818
105	C1+	2310	-1145	142	DUMMY	4900	-1145	179	DUMMY	5166	884
106	C1+	2380	-1145	143	DUMMY	4970	-1145	180	DUMMY	5166	964
107	C2+	2450	-1145	144	DUMMY	5166	-964	181	DUMMY	5060	1136
108	C2+	2520	-1145	145	COM63	5166	-898	182	DUMMY	4980	1136
109	C2-	2590	-1145	146	COM62	5166	-846	183	COM29	4914	1136
110	C2-	2660	-1145	147	COM61	5166	-794	184	COM28	4862	1136
111	C4+	2730	-1145	148	COM60	5166	-742	185	COM27	4810	1136
112	C4+	2800	-1145	149	COM59	5166	-690	186	COM26	4758	1136
113	VDD	2870	-1145	150	COM58	5166	-638	187	COM25	4706	1136
114	VDD	2940	-1145	151	COM57	5166	-586	188	COM24	4654	1136
115	REF	3010	-1145	152	COM56	5166	-534	189	COM23	4602	1136
116	VSS	3080	-1145	153	COM55	5166	-482	190	COM22	4550	1136
117	VEXT	3150	-1145	154	COM54	5166	-430	191	COM21	4498	1136
118	VDD	3220	-1145	155	COM53	5166	-378	192	COM20	4446	1136
119	INTRS	3290	-1145	156	COM52	5166	-326	193	COM19	4394	1136
120	VSS	3360	-1145	157	COM51	5166	-274	194	COM18	4342	1136
121	VSS	3430	-1145	158	COM50	5166	-222	195	COM17	4290	1136
122	V4	3500	-1145	159	COM49	5166	-170	196	COM16	4238	1136
123	V4	3570	-1145	160	COM48	5166	-118	197	COM15	4186	1136
124	V3	3640	-1145	161	COM47	5166	-66	198	COM14	4134	1136
125	V3	3710	-1145	162	COM46	5166	-14	199	COM13	4082	1136
126	V3	3780	-1145	163	COM45	5166	38	200	COM12	4030	1136
127	V3	3850	-1145	164	COM44	5166	90	201	COM11	3978	1136
128	V1	3920	-1145	165	COM43	5166	142	202	COM10	3926	1136
129	V1	3990	-1145	166	COM42	5166	194	203	COM9	3874	1136
130	V0	4060	-1145	167	COM41	5166	246	204	COM8	3822	1136
131	V0	4130	-1145	168	COM40	5166	298	205	COM7	3770	1136
132	VR	4200	-1145	169	COM39	5166	350	206	COM6	3718	1136
133	VR	4270	-1145	170	COM38	5166	402	207	COM5	3666	1136
134	VSS	4340	-1145	171	COM37	5166	454	208	COM4	3614	1136
135	VSS	4410	-1145	172	COM36	5166	506	209	COM3	3562	1136
136	VDD	4480	-1145	173	COM35	5166	558	210	COM2	3510	1136
137	OSC1	4550	-1145	174	COM34	5166	610	211	COM1	3458	1136
138	DUMMY	4620	-1145	175	COM33	5166	662	212	COM0	3406	1136
139	DUMMY	4690	-1145	176	COM32	5166	714	213	DUMMY	3354	1136

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y
214	SEG0	3302	1136	249	SEG35	1482	1136	284	SEG70	-338	1136
215	SEG1	3250	1136	250	SEG36	1430	1136	285	SEG71	-390	1136
216	SEG2	3198	1136	251	SEG37	1378	1136	286	SEG72	-442	1136
217	SEG3	3146	1136	252	SEG38	1326	1136	287	SEG73	-494	1136
218	SEG4	3094	1136	253	SEG39	1274	1136	288	SEG74	-546	1136
219	SEG5	3042	1136	254	SEG40	1222	1136	289	SEG75	-598	1136
220	SEG6	2990	1136	255	SEG41	1170	1136	290	SEG76	-650	1136
221	SEG7	2938	1136	256	SEG42	1118	1136	291	SEG77	-702	1136
222	SEG8	2886	1136	257	SEG43	1066	1136	292	SEG78	-754	1136
223	SEG9	2834	1136	258	SEG44	1014	1136	293	SEG79	-806	1136
224	SEG10	2782	1136	259	SEG45	962	1136	294	SEG80	-858	1136
225	SEG11	2730	1136	260	SEG46	910	1136	295	SEG81	-910	1136
226	SEG12	2678	1136	261	SEG47	858	1136	296	SEG82	-962	1136
227	SEG13	2626	1136	262	SEG48	806	1136	297	SEG83	-1014	1136
228	SEG14	2574	1136	263	SEG49	754	1136	298	SEG84	-1066	1136
229	SEG15	2522	1136	264	SEG50	702	1136	299	SEG85	-1118	1136
230	SEG16	2470	1136	265	SEG51	650	1136	300	SEG86	-1170	1136
231	SEG17	2418	1136	266	SEG52	598	1136	301	SEG87	-1222	1136
232	SEG18	2366	1136	267	SEG53	546	1136	302	SEG88	-1274	1136
233	SEG19	2314	1136	268	SEG54	494	1136	303	SEG89	-1326	1136
234	SEG20	2262	1136	269	SEG55	442	1136	304	SEG90	-1378	1136
235	SEG21	2210	1136	270	SEG56	390	1136	305	SEG91	-1430	1136
236	SEG22	2158	1136	271	SEG57	338	1136	306	SEG92	-1482	1136
237	SEG23	2106	1136	272	SEG58	286	1136	307	SEG93	-1534	1136
238	SEG24	2054	1136	273	SEG59	234	1136	308	SEG94	-1586	1136
239	SEG25	2002	1136	274	SEG60	182	1136	309	SEG95	-1638	1136
240	SEG26	1950	1136	275	SEG61	130	1136	310	SEG96	-1690	1136
241	SEG27	1898	1136	276	SEG62	78	1136	311	SEG97	-1742	1136
242	SEG28	1846	1136	277	SEG63	26	1136	312	SEG98	-1794	1136
243	SEG29	1794	1136	278	SEG64	-26	1136	313	SEG99	-1846	1136
244	SEG30	1742	1136	279	SEG65	-78	1136	314	SEG100	-1898	1136
245	SEG31	1690	1136	280	SEG66	-130	1136	315	SEG101	-1950	1136
246	SEG32	1638	1136	281	SEG67	-182	1136	316	SEG102	-2002	1136
247	SEG33	1586	1136	282	SEG68	-234	1136	317	SEG103	-2054	1136
248	SEG34	1534	1136	283	SEG69	-286	1136	318	SEG104	-2106	1136

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y
319	SEG105	-2158	1136	354	COM76	-3978	1136	389	COM107	-5166	194
320	SEG106	-2210	1136	355	COM77	-4030	1136	390	COM108	-5166	142
321	SEG107	-2262	1136	356	COM78	-4082	1136	391	COM109	-5166	90
322	SEG108	-2314	1136	357	COM79	-4134	1136	392	COM110	-5166	38
323	SEG109	-2366	1136	358	COM80	-4186	1136	393	COM111	-5166	-14
324	SEG110	-2418	1136	359	COM81	-4238	1136	394	COM112	-5166	-66
325	SEG111	-2470	1136	360	COM82	-4290	1136	395	COM113	-5166	-118
326	SEG112	-2522	1136	361	COM83	-4342	1136	396	COM114	-5166	-170
327	SEG113	-2574	1136	362	COM84	-4394	1136	397	COM115	-5166	-222
328	SEG114	-2626	1136	363	COM85	-4446	1136	398	COM116	-5166	-274
329	SEG115	-2678	1136	364	COM86	-4498	1136	399	COM117	-5166	-326
330	SEG116	-2730	1136	365	COM87	-4550	1136	400	COM118	-5166	-378
331	SEG117	-2782	1136	366	COM88	-4602	1136	401	COM119	-5166	-430
332	SEG118	-2834	1136	367	COM89	-4654	1136	402	COM120	-5166	-482
333	SEG119	-2886	1136	368	COM90	-4706	1136	403	COM121	-5166	-534
334	SEG120	-2983	1136	369	COM91	-4758	1136	404	COM122	-5166	-586
335	SEG121	-2990	1136	370	COM92	-4810	1136	405	COM123	-5166	-638
336	SEG122	-3042	1136	371	COM93	-4862	1136	406	COM124	-5166	-690
337	SEG123	-3094	1136	372	COM94	-4914	1136	407	COM125	-5166	-740
338	SEG124	-3146	1136	373	DUMMY	-4980	1136	408	COM126	-5166	-794
339	SEG125	-3198	1136	374	DUMMY	-5060	1136	409	COM127	-5166	-846
340	SEG126	-3250	1136	375	DUMMY	-5166	964	410	COMS1	-5166	-898
341	SEG127	-3302	1136	376	DUMMY	-5166	884	411	DUMMY	-5166	-964
342	COM64	-3354	1136	377	COM95	-5166	818				
343	COM65	-3406	1136	378	COM96	-5166	76				
344	COM66	-3458	1136	379	COM97	-5166	714				
345	COM67	-3510	1136	380	COM98	-5166	662				
346	COM68	-3562	1136	381	COM99	-5166	610				
347	COM69	-3614	1136	382	COM100	-5166	558				
348	COM70	-3666	1136	383	COM101	-5166	506				
349	COM71	-3718	1136	384	COM102	-5166	454				
350	COM72	-3770	1136	385	COM103	-5166	402				
351	COM73	-3822	1136	386	COM104	-5166	350				
352	COM74	-3874	1136	387	COM105	-5166	298				
353	COM75	-3926	1136	388	COM106	-5166	246				

PIN DESCRIPTION

POWER SUPPLY

Table 3. Power Supply Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>V_{DD}</td><td>Supply</td><td>Power supply</td></tr>
<tr><td>V_{SS}</td><td>Supply</td><td>Ground</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>LCD driver supply voltages
The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.
Voltages should have the following relationship;
$V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V_{SS}$
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.
<table>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/N bias</td><td>(N-1)/N x V0</td><td>(N-2)/N x V0</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
<tr><td colspan="5">NOTE: N = 5 to 12</td></tr>
</table>
</td></tr>
</table>

LCD DRIVER SUPPLY

Table 4. LCD Driver Supply Pin Description

Name	I/O	Description
C1-	O	Capacitor 1 negative connection pin for voltage converter
C1+	O	Capacitor 1 positive connection pin for voltage converter
C2-	O	Capacitor 2 negative connection pin for voltage converter
C2+	O	Capacitor 2 positive connection pin for voltage converter
C3+	O	Capacitor 3 positive connection pin for voltage converter
C4+	O	Capacitor 4 positive connection pin for voltage converter
C5+	O	Capacitor 5 positive connection pin for voltage converter
VOUT	I/O	Voltage converter input/output pin
VCI	I	Voltage converter input voltage pin
VR	I	V0 voltage adjustment pin It is valid only when on-chip resistors are not used (INTRS = "L") When using internal resistors (INTRS = "H"), open this pin
REF	I	Selects the external VREF voltage via the VEXT pin – REF = "H": using the internal VREF – REF = "L": using the external VREF
VEXT	I	Externally input reference voltage (VREF) for the internal voltage regulator It is valid only when REF is "L" When using internal voltage regulator, connect to VDD, VSS or open this pin
OSC1	I	When using internal clock oscillator, connect a resistor between OSC1 and VDD.

SYSTEM CONTROL

Table 5. System Control Pin Description

Name	I/O	Description
INTRS	I	Internal resistor select pin This pin selects the resistors for adjusting V0 voltage level – INTRS = "H": use the internal resistors. – INTRS = "L": use the external resistors VR pin and external resistive divider control V0 voltage
TEST1	O	Test pins Don' t use this pin. – TEST1: Open this pin.

MICROPROCESSOR INTERFACE

Table 6. Microprocessor Interface Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESETB</td><td>I</td><td>Reset input pin
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td>PS0</td><td>I</td><td>Parallel/Serial data input select input
<table>
<tr><th>PS0</th><th>Interface mode</th><th>Data/instruction</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>H</td><td>Parallel</td><td>RS</td><td>DB0 to DB7</td><td>E_RD
RW_WR</td><td>–</td></tr>
<tr><td>L</td><td>Serial</td><td>RS or None</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
<tr><td colspan="6">NOTE: In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either “H” or “L”.</td></tr>
</table></td></tr>
<tr><td>PS1</td><td>I</td><td>Microprocessor interface select input pin
– PS0 = “H”, PS1 = "H": 6800-series parallel MPU interface
– PS0 = “H”, PS1 = "L": 8080-series parallel MPU interface
– PS0 = “L”, PS1 = "H": 4 pin-SPI MPU interface
– PS0 = “L”, PS1 = "L": 3 pin-SPI MPU interface</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CSB is "L". When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin
– RS = "H": DB0 to DB7 are display data – RS = "L": DB0 to DB7 are control data</td></tr>
<tr><td>RW_WR</td><td>I</td><td>Read/Write execution control pin
<table>
<tr><th>C68</th><th>MPU type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read/Write control input pin
– RW = “H” : read – RW = “L” : write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
<tr><td>E_RD</td><td>I</td><td>Read/Write execution control pin
<table>
<tr><th>PS1</th><th>MPU Type</th><th>E_RD</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin
– RW = “H”: When E is “H”, DB0 to DB7 are in an output status.
– RW = “L”: The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, DB0 to DB7 are in an output status.</td></tr>
</table></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td>8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus.
When the serial interface selected (PS0 = "L");
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
</table>

LCD DRIVER OUTPUTS

Table 7. LCD Driver Output Pin Description

Name	I/O	Description			
SEG0-SEG127	O	LCD segment driver outputs The display data and the M signal control the output voltage of segment driver.			
		Display data	M (Internal)	Segment driver output voltage	
				Normal display	Reverse display
		H	H	V0	V2
		H	L	V_{SS}	V3
		L	H	V2	V0
		L	L	V3	V_{SS}
		Power save mode		V_{SS}	V_{SS}
COM0-COM127	O	LCD common driver outputs The internal scanning data and M signal control the output voltage of common driver.			
		Scan data	M (Internal)	Common driver output voltage	
		H	H	V_{SS}	
		H	L	V0	
		L	H	V1	
		L	L	V4	
		Power save mode		VSS	
COMS (COMS1)	O	Common output for the icons The output signals of two pins are same. When not used, these pins should be left open.			

NOTE: DUMMY —These pins should be opened (floated).

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There is CSB pin for chip selection. The S6B0741 can interface with an MPU when CSB is "L". When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel/Serial Interface

S6B0741 has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in Table 8.

Table 8. Parallel/Serial Interface Mode

Type	PS1	CSB	PS0	Interface mode
Parallel	H	CSB	H	6800-series MPU mode
	L			8080-series MPU mode
Serial	H	CSB	L	4-pin SPI mode
	L			3-pin SPI mode

Parallel Interface (PS0 = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS1 as shown in Table 9. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in Table 10.

Table 9. Microprocessor Selection for Parallel Interface

PS1	CSB	RS	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CSB	RS	E	RW	DB0 to DB7	6800-series
L	CSB	RS	/RD	/WR	DB0 to DB7	8080-series

Table 10. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

NOTE: When E_RD pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at RS, RW_WR as in case of 6800-series mode.

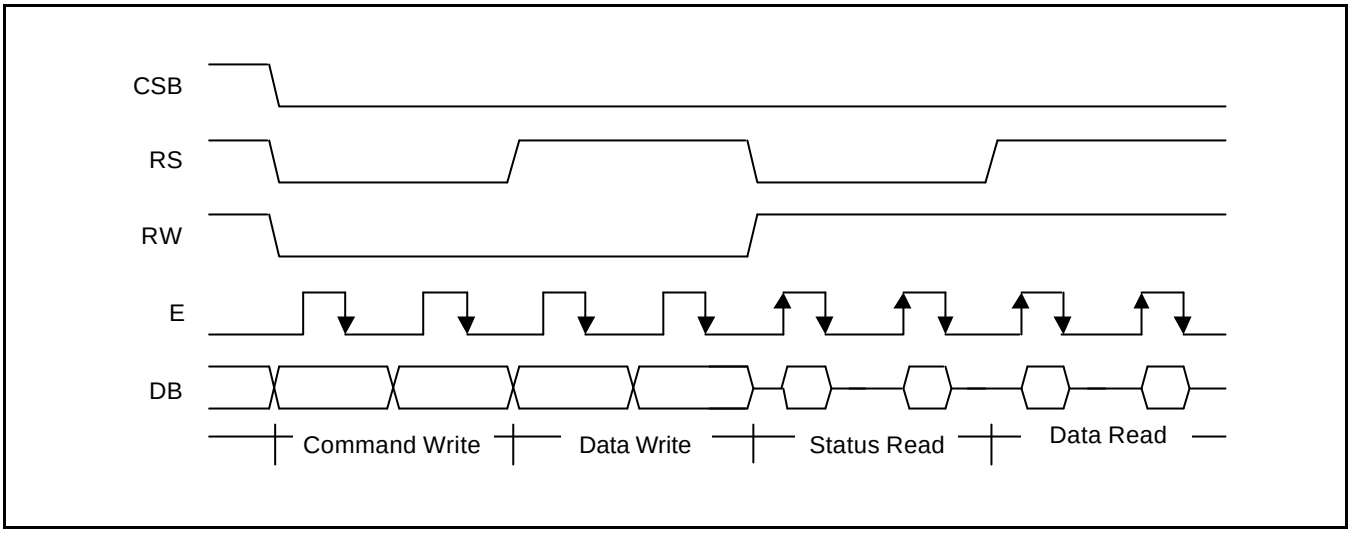


Figure 3. 6800-Series MPU Interface protocol (PS0="H", PS1="H")

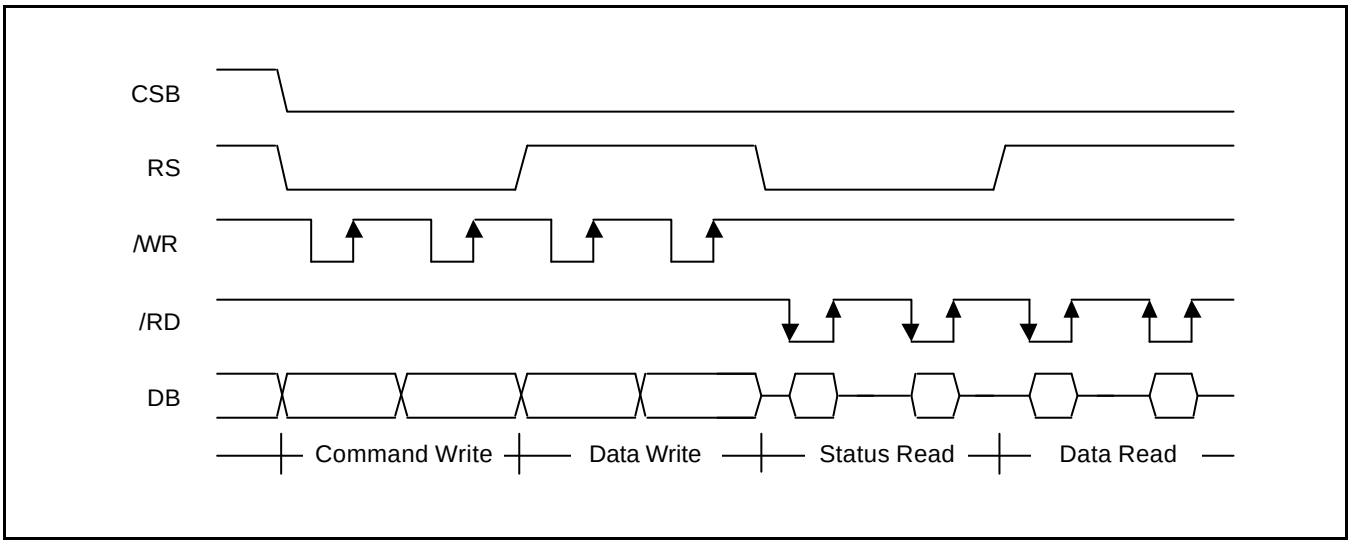


Figure 4. 8080-Series MPU Interface Protocol (PS0="H", PS1="L")

Serial Interface (PS0 = "L")

When the S6B0741 is active(CSB="L"), serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either via software or the Register Select(RS) Pin, based on the setting of PS1. When the RS pin is used (PS1 = "H"), data is display data when RS is high, and command data when RS is low. When RS is not used (PS1 = "L"), the LCD Driver will receive command from MCU by default. If messages on the data pin are data rather than command, MCU should send Data Direction command(11101000) to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are send, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string is handled as command data.

Serial mode	PS0	PS1	CSB	RS
4-Pin SPI mode	L	H	CSB	Used
3-Pin SPI mode	L	L	CSB	Not used

4-pin SPI Mode (PS0 = "L" , PS1 = "H")

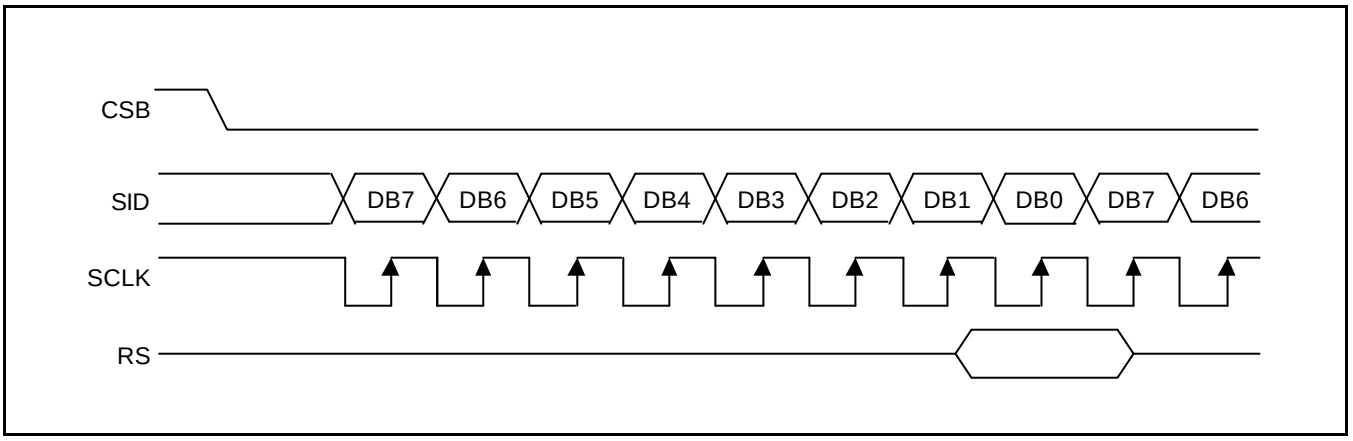


Figure 5. 4-pin SPI Timing (RS is used)

3-pin SPI Mode (PS0 = "L" , PS1 = "L")

To write data to the DDRAM, send Data Direction Command in 3-pin SPI mode. Data is latched at the rising edge of SCLK. And the DDRAM column address pointer will be increased by one automatically.

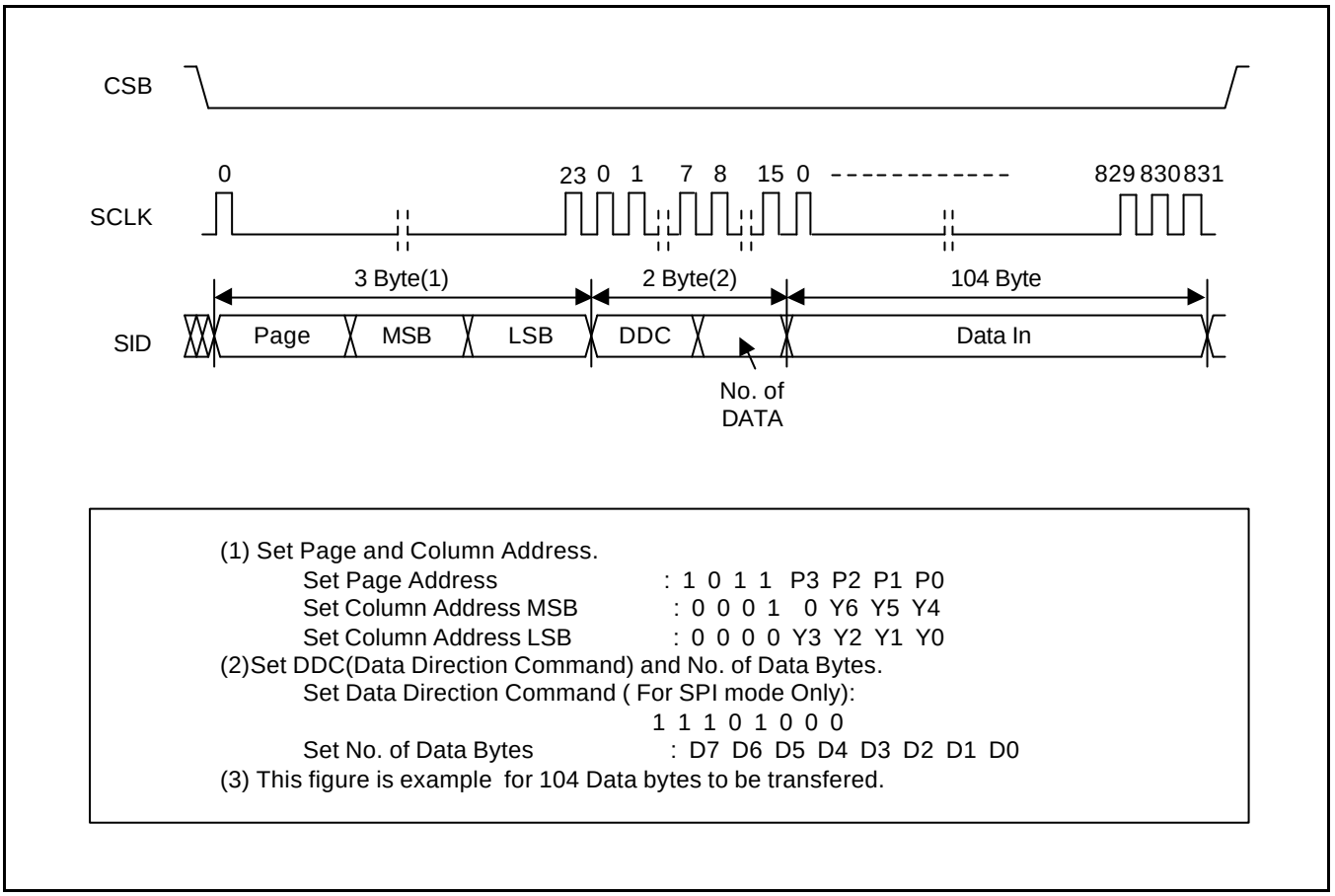


Figure 6. 3-pin SPI Timing (RS is not used)

This command is used in 3-pin SPI mode only. It will be two continuous commands, the first byte controls the data direction and informs the LCD driver the second byte will be number of data bytes will be write. After these two commands sending out, the following messages will be data. If data is stopped in transmitting, it is not valid data. New data will be transferred serially with most significant bit first.

NOTE: In spite of transmission of data, if CSB will be disable, state terminates abnormally. Next state is initialized.

Busy Flag

The Busy Flag indicates whether the S6B0741 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The S6B0741 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Figure 7. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 6. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

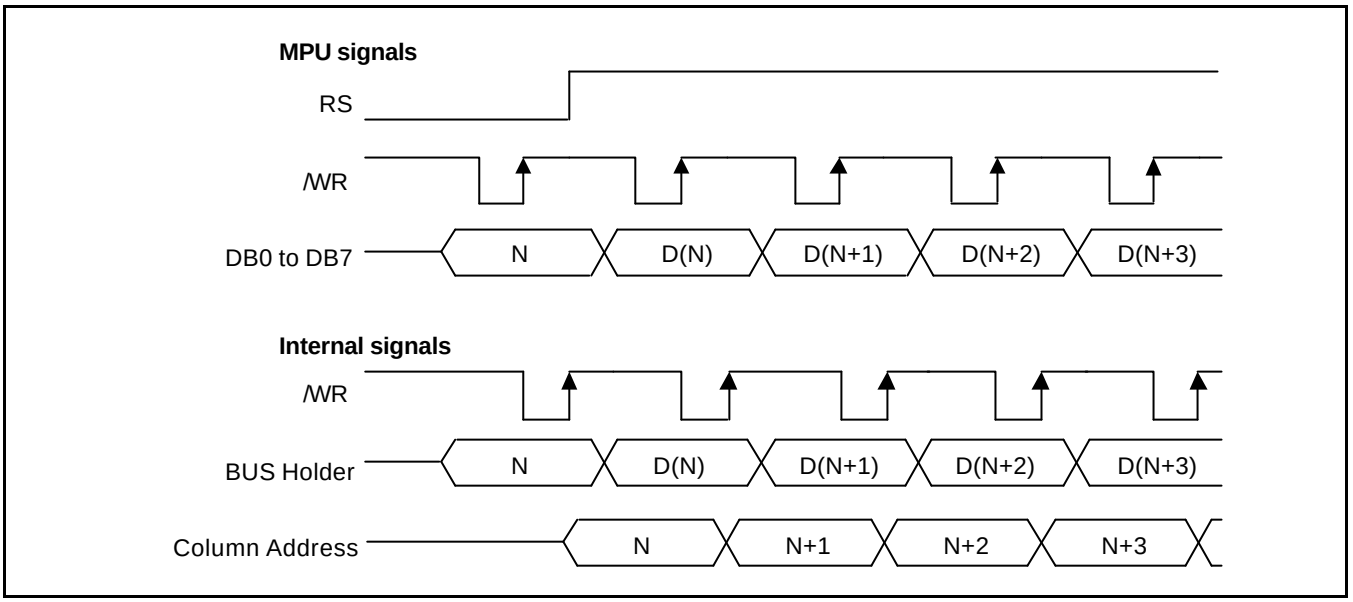


Figure 7. Write Timing

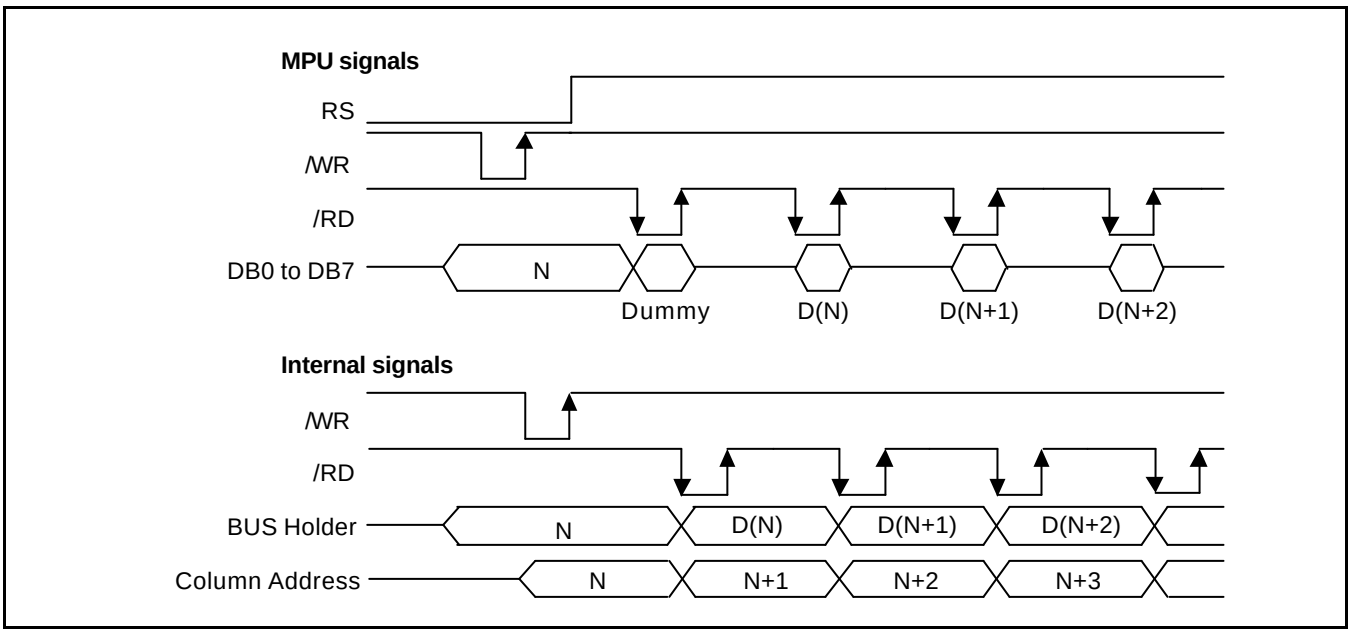


Figure 8. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 129-row (17 page by 8 bits) by 128-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 129 rows are divided into 16 pages of 8 lines and the 17th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in Figure 10. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 16 is a special RAM area for the icons and display data DB0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 10. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 128-bit RAM data to the display data latch circuit. When icon is enabled by setting icon control register, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

Column Address Circuit has a 8-bit preset counter that provides Column Address to the Display Data RAM as shown in figure 10. When set Column Address MSB/LSB instruction is issued, 7-bit [Y7:Y1] are set and lowest bit, Y0 is set to "0". Since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 80H. It is unlocked if a column address is set again by set Column Address MSB/LSB instruction. And the column address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following Figure 9.

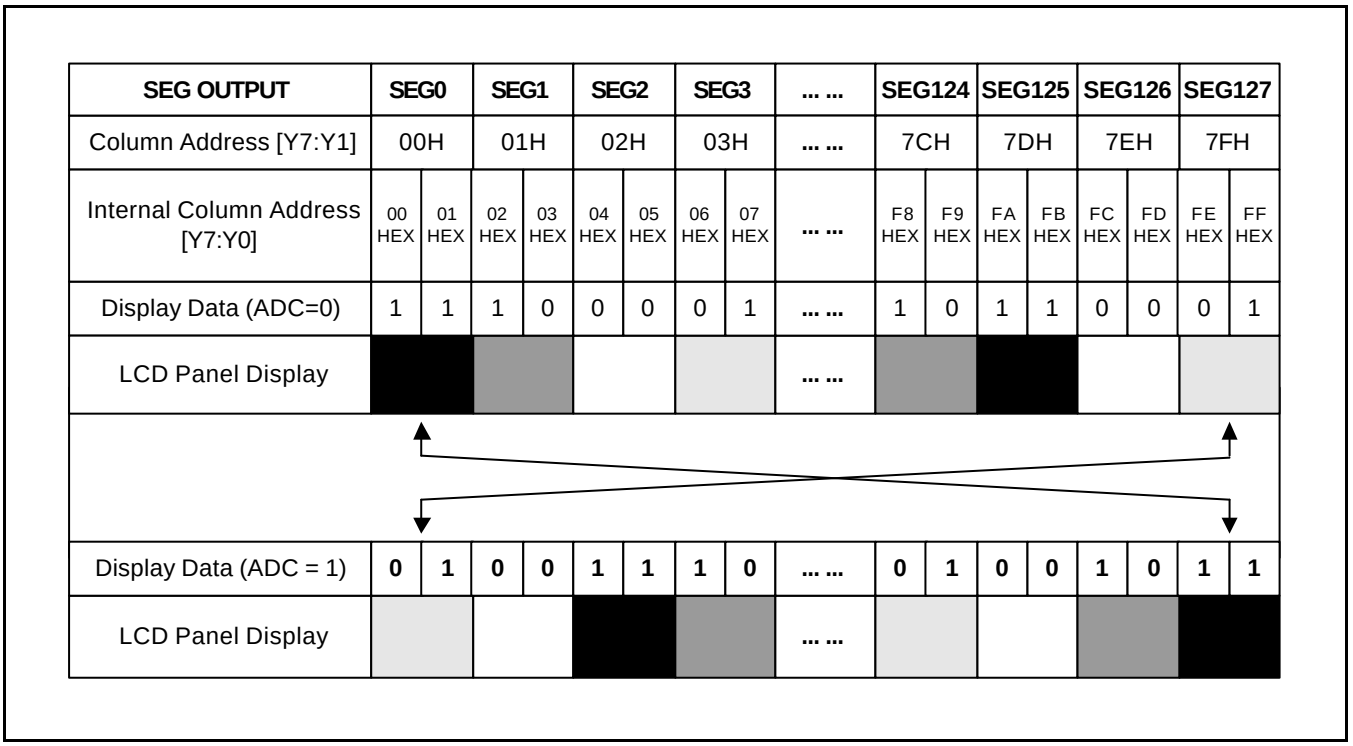


Figure 9. The Relationship between the Column Address and the Segment Outputs

Segment Control Circuit

This circuit controls the display data by the display ON/OFF, reverse display ON/OFF and entire display ON/OFF instructions without changing the data in the display data RAM.

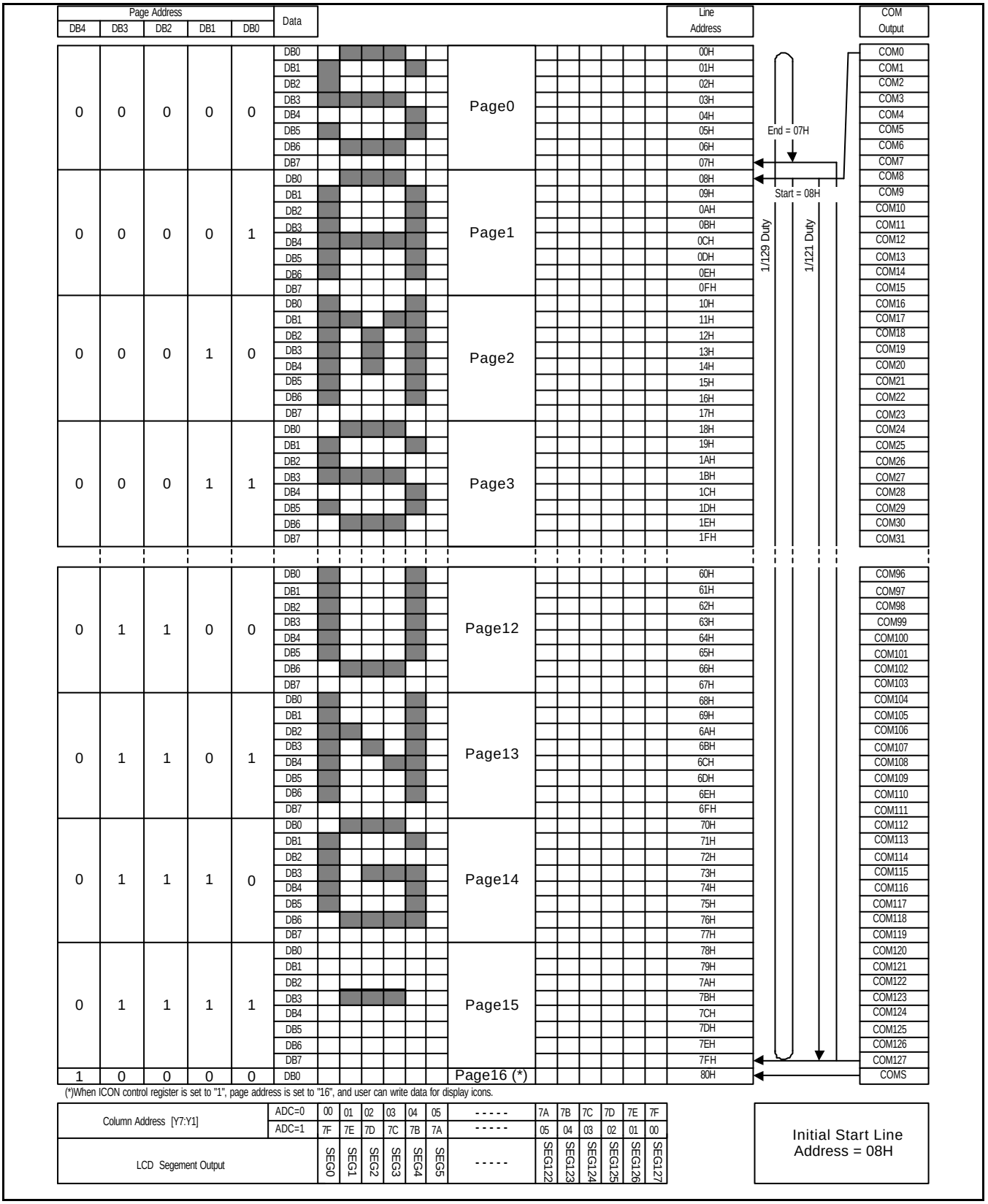


Figure 10. Display Data RAM Map

SAMSUNG ELECTRONICS

LCD DISPLAY CIRCUITS

FRC (Frame Rate Control) and PWM (Pulse Width Modulation) Function Circuit

The S6B0741 incorporates an FRC function and a PWM function circuit to display a 4-level gray scale. The FRC function and PWM utilize liquid crystal characteristics whose transmission is changed by an effective value of applied voltage. The S6B0741 provides four 4-bit palette-registers to assign the desired gray level. These registers are set by the instructions and the RESETB.

— Gray Scale Table of 4 FRC (Frame Rate Control)

Gray scale level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Light gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Dark gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)

— Gray Scale Table of 3 FRC (Frame Rate Control)

Gray scale level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)
Light gray	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)
Dark gray	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)

— **Gray Scale Table of 15 PWM (Pulse Width Modulation)**

Dec	Hex	4-bits	PWM (on width)	Note
0	00	0000	0 (0/15)	Brighter
1	01	0001	1/15	
2	02	0010	2/15	
3	03	0011	3/15	
4	04	0100	4/15	
5	05	0101	5/15	
6	06	0110	6/15	
7	07	0111	7/15	
8	08	1000	8/15	
9	09	1001	9/15	
10	0A	1010	10/15	
11	0B	1011	11/15	
12	0C	1100	12/15	
13	0D	1101	13/15	
14	0E	1110	14/15	
15	0F	1111	1 (15/15)	Darker

— **Gray Scale Table of 12 PWM (Pulse Width Modulation)**

Dec	Hex	4-bits	PWM (on width)	Note
0	00	0000	0 (0/12)	Brighter
1	01	0001	1/12	
2	02	0010	2/12	
3	03	0011	3/12	
4	04	0100	4/12	
5	05	0101	5/12	
6	06	0110	6/12	
7	07	0111	7/12	
8	08	1000	8/12	
9	09	1001	9/12	
10	0A	1010	10/12	
11	0B	1011	11/12	
12	0C	1100	1 (12/12)	Darker
13	0D	1101	0/12	This area is selected to OFF level (0/12 level)
14	0E	1110	0/12	
15	0F	1111	0/12	

— **Gray Scale Table of 9 PWM (Pulse Width Modulation)**

Dec	Hex	4-bits	PWM (on width)	Note
0	00	0000	0 (0/9)	Brighter
1	01	0001	1/9	
2	02	0010	2/9	
3	03	0011	3/9	
4	04	0100	4/9	
5	05	0101	5/9	
6	06	0110	6/9	
7	07	0111	7/9	
8	08	1000	8/9	
9	09	1001	1 (9/9)	Darker
10	0A	1010	0/9	This area is selected
11	0B	1011	0/9	to OFF level (0/9 level)
12	0C	1100	0/9	
13	0D	1101	0/9	
14	0E	1110	0/9	
15	0F	1111	0/9	

Oscillator

This is on-chip Oscillator with external resistor. Its frequency is controlled by external resistor between OSC1 and V_{DD}. This oscillator signal is used in the voltage converter and display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL(internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 128-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 11.

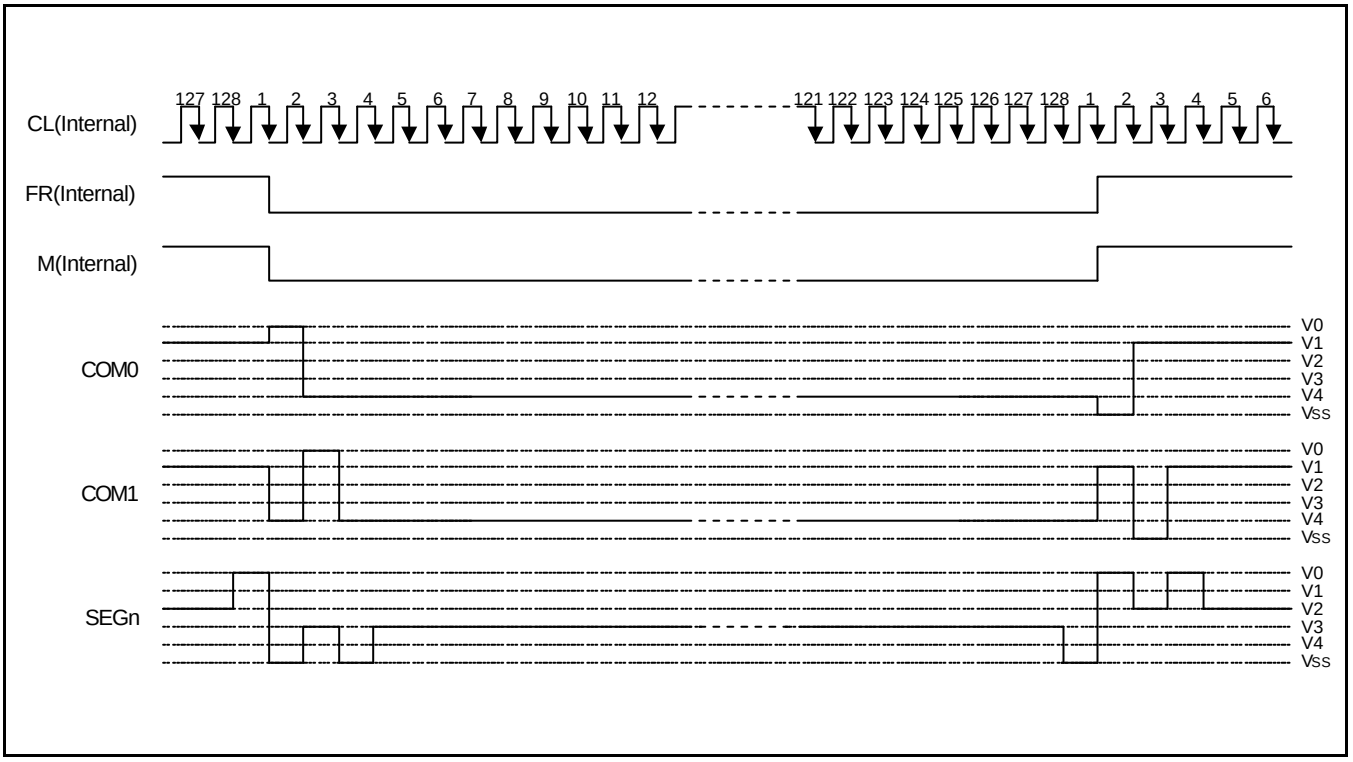


Figure 11. 2-frame AC Driving Waveform (Duty Ratio = 1/128)

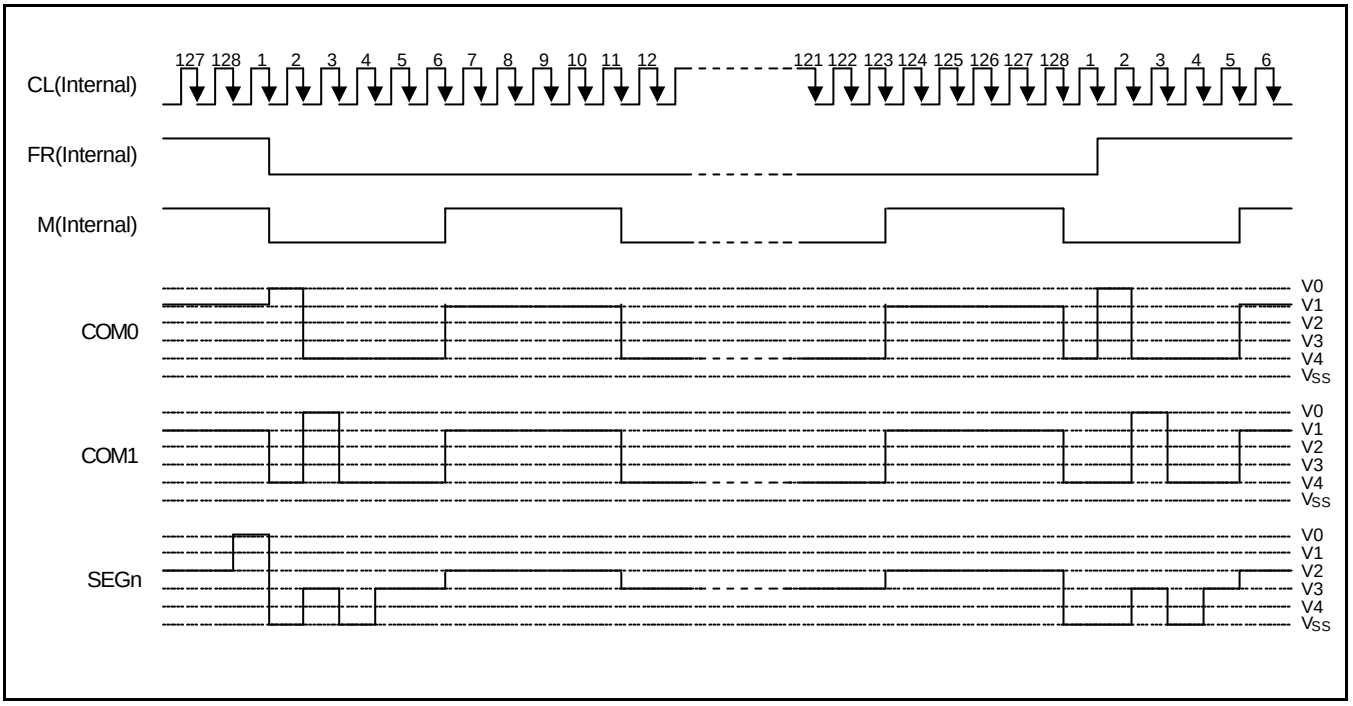


Figure 12. N-Line Inversion Driving Waveform (N = 5, Duty Ratio = 1/128)

LCD DRIVER CIRCUIT

This driver circuit is configured by 129-channel common drivers and 128-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.

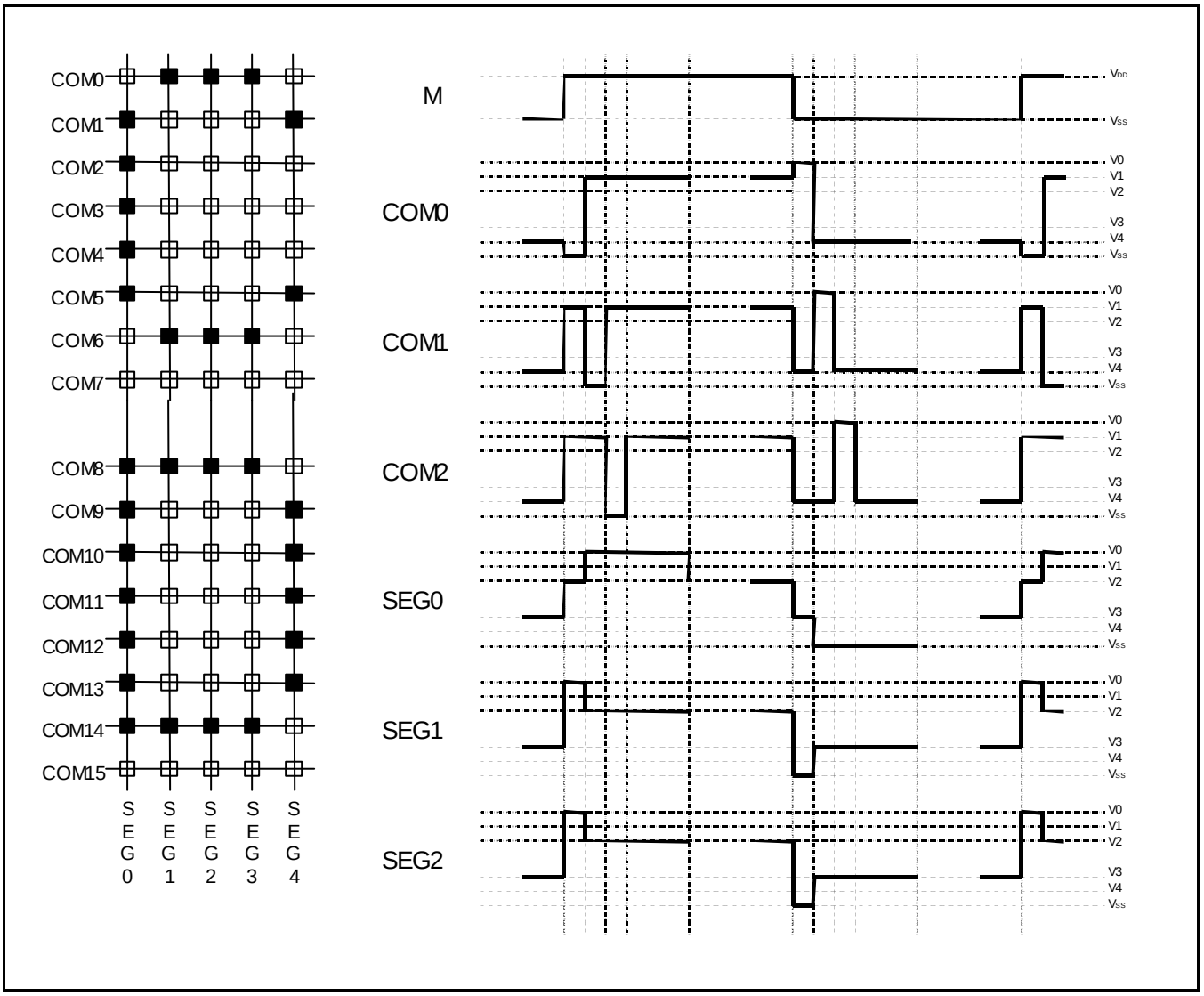


Figure 13. Segment and Common Timing

Partial Display on LCD

The S6B0741 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages

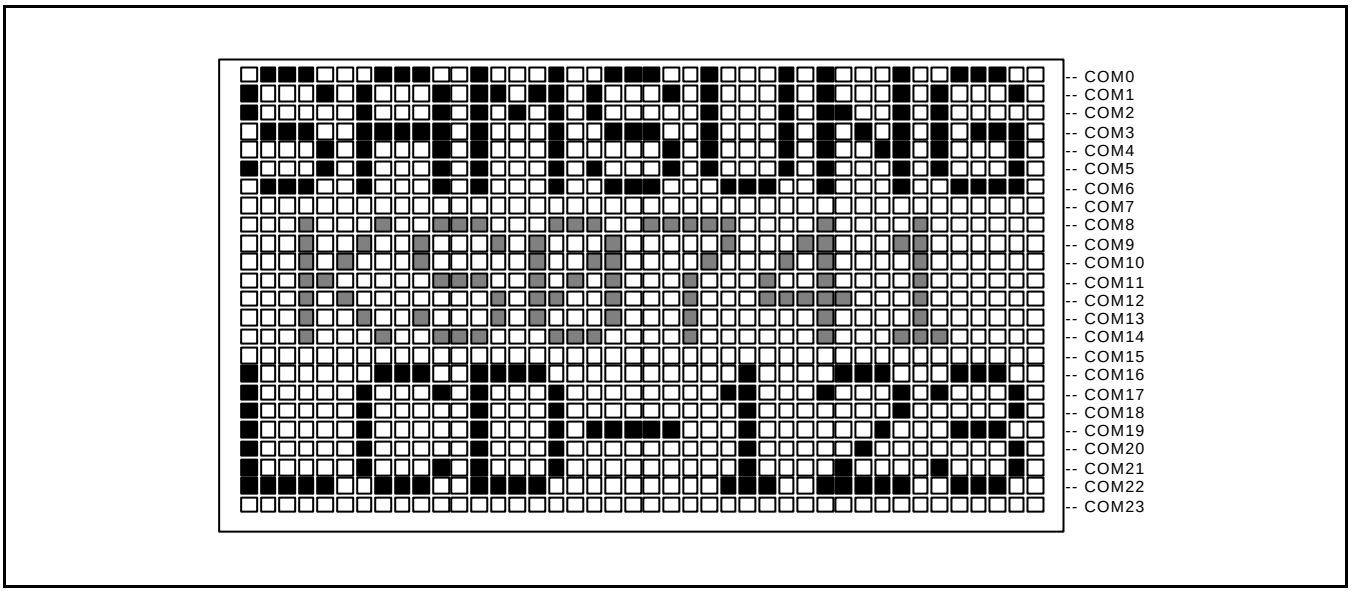


Figure 14. Reference Example for Partial Display

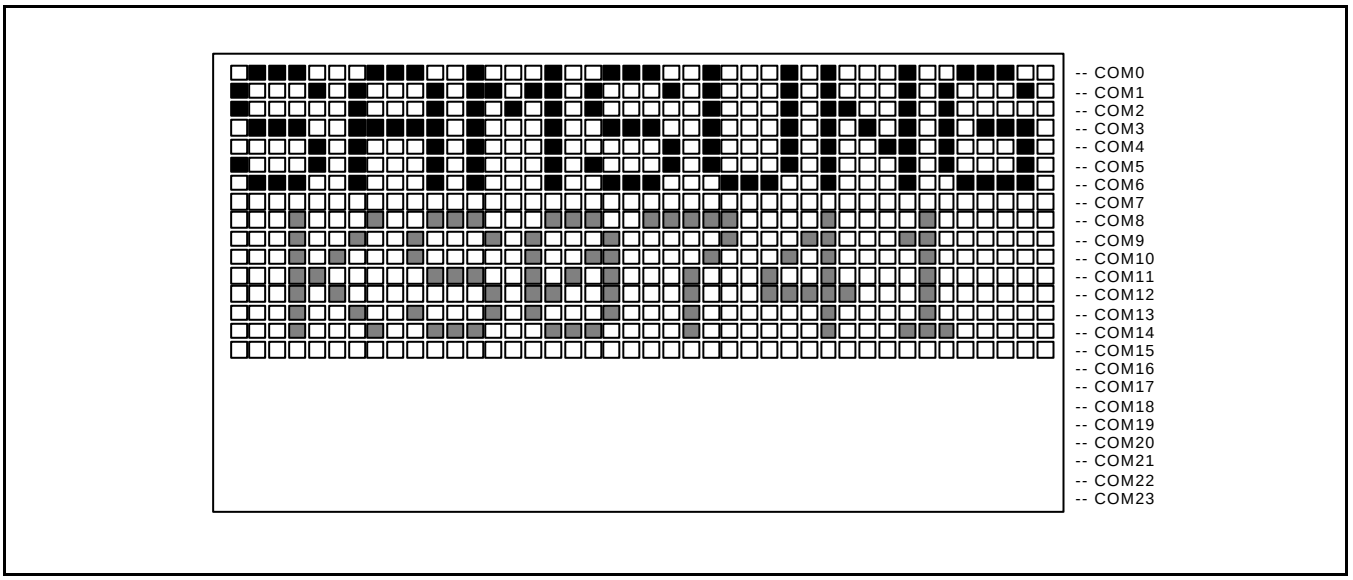


Figure 15. Partial Display (Partial Display Duty = 16, Initial COM0 = 0)

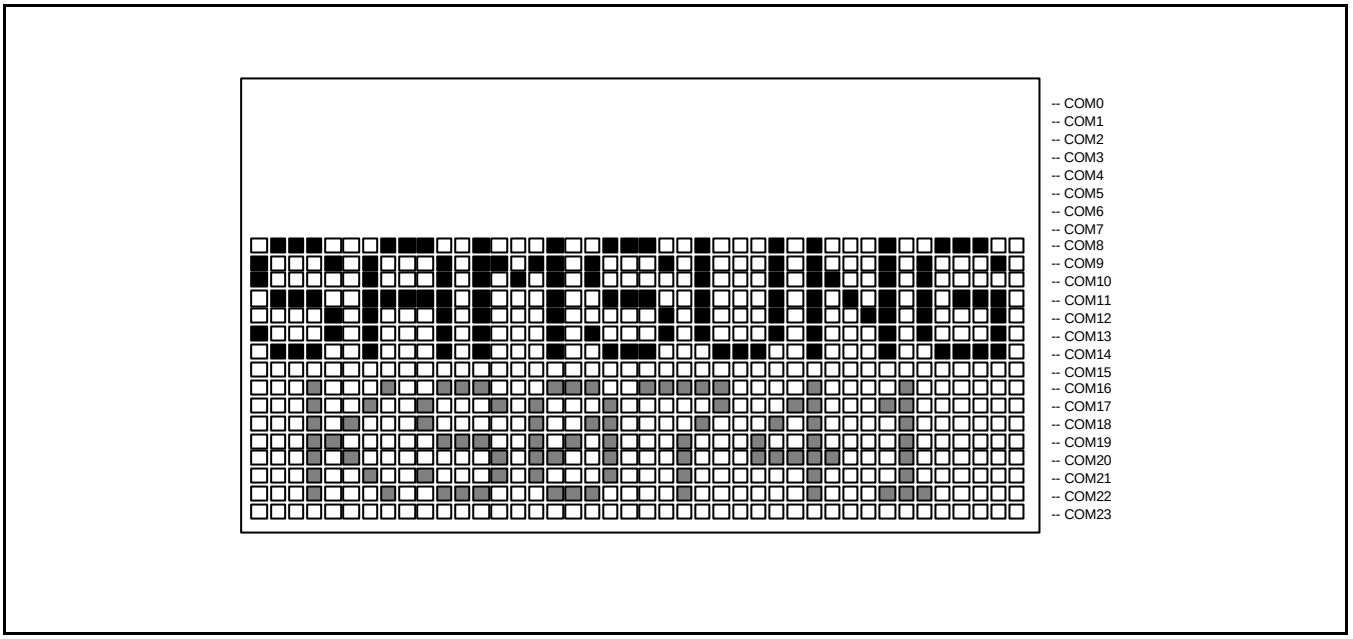


Figure 16. Moving Display (Partial Display Duty = 16, Initial COM0 = 8)

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 11 shows the referenced combinations in using Power Supply circuits.

Table 11. Recommended Power Supply Combinations

User setup	Power ontrol (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VCI and V_{SS} to 3, 4, 5 or 6 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by "Set DC-DC Step-up" instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

[C1 = 1.0 to 4.7 *m*F]

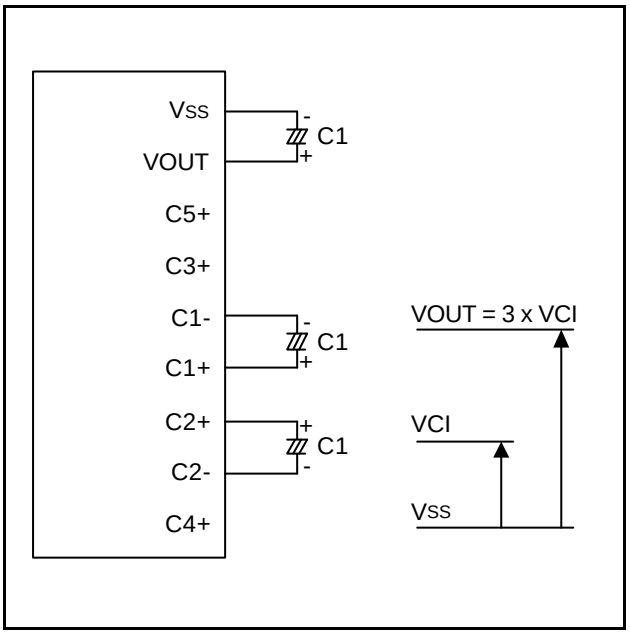


Figure 17. Three Times Boosting Circuit

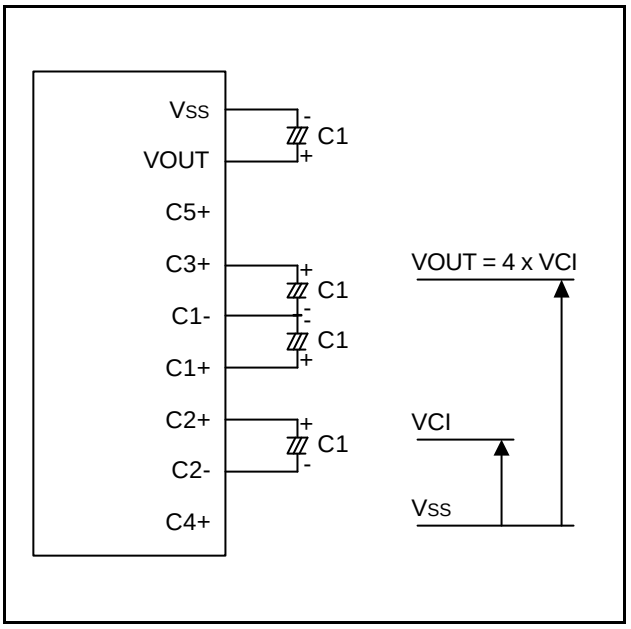


Figure 18. Four Times Boosting Circuit

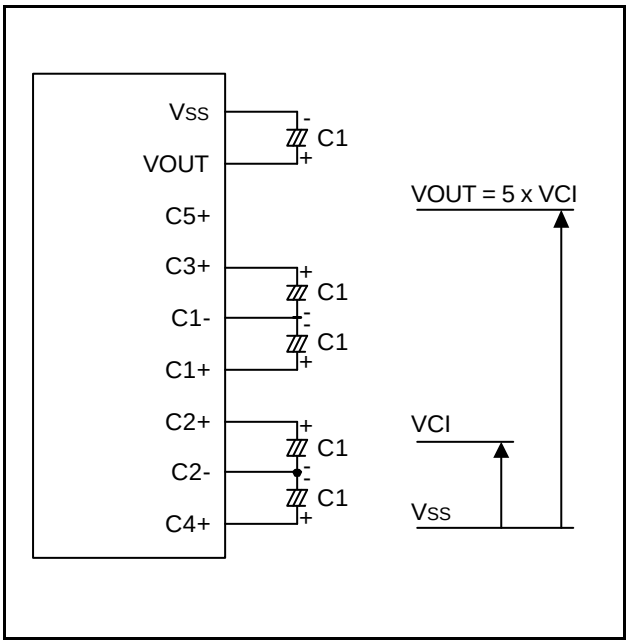


Figure 19. Five Times Boosting Circuit

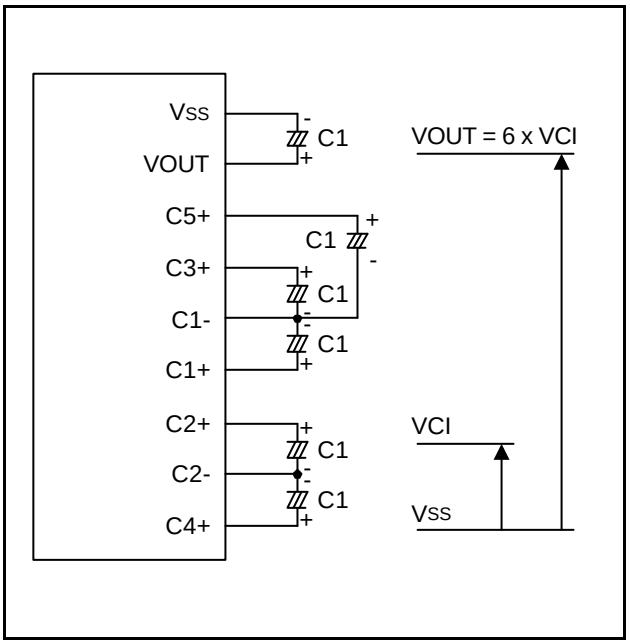


Figure 20. Six Times Boosting Circuit

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Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in figure 19, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And VEV called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta= 25°C is shown in Table 12.

$$V0 = (1 + \frac{Rb}{Ra}) \times V_{EV} \text{ [V]} \text{ ------ (Eq.1)}$$

$$V_{EV} = (1 - \frac{(63 - \alpha)}{210}) \times V_{REF} \text{ [V]} \text{ ------ (Eq.2)}$$

Table 12 . V_{REF} Voltage at Ta = 25°C

REF	Temp. coefficient	VREF [V]
1	-0.125%/°C	2.1
0	External input	VEXT

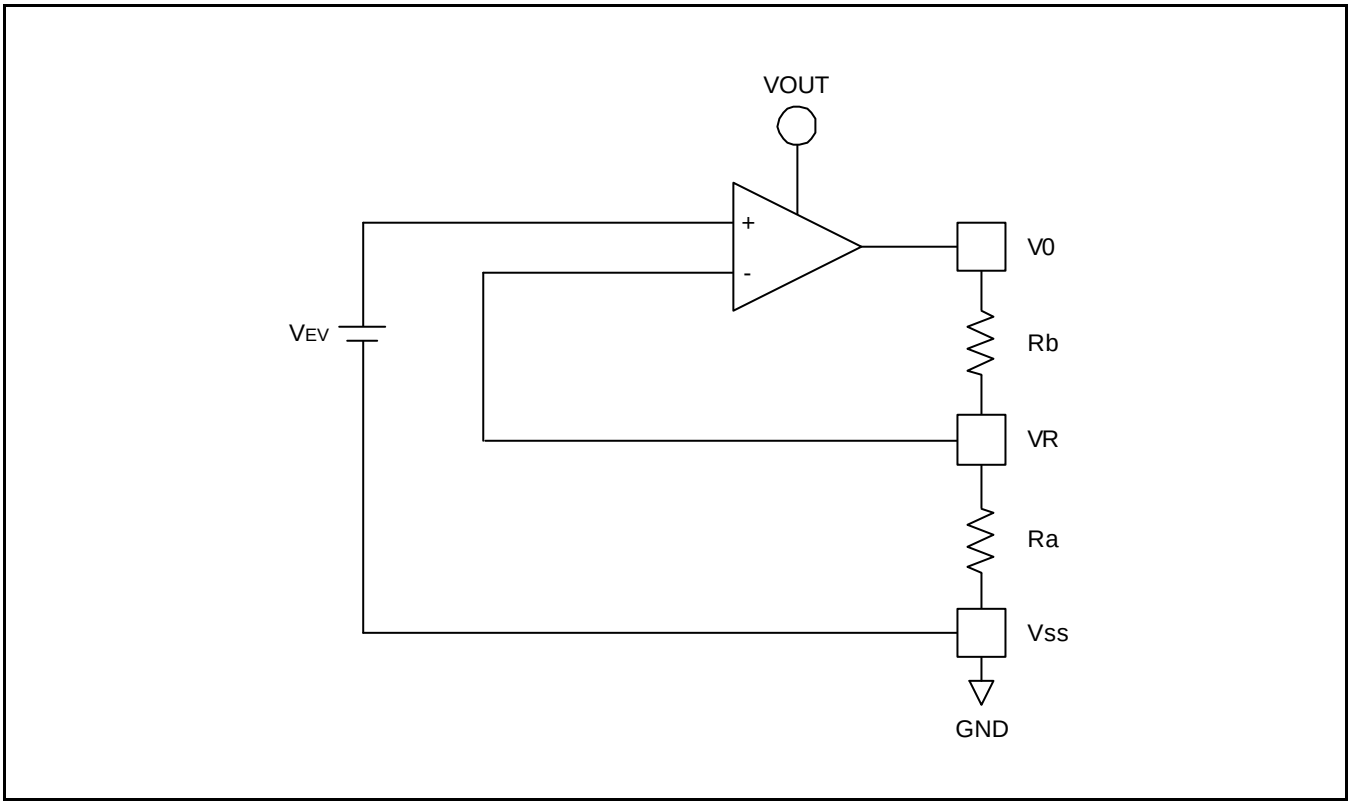

Figure 21. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is "H", resistor Ra is connected internally between VR pin and V_{SS}, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 13. Internal Rb/Ra Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1 + (Rb/Ra)	2.3	3.0	3.7	4.4	5.1	5.8	6.5	7.2

Figure 22 Shows V0 voltage measured by adjusting internal regulator resistor ratio (Rb/Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

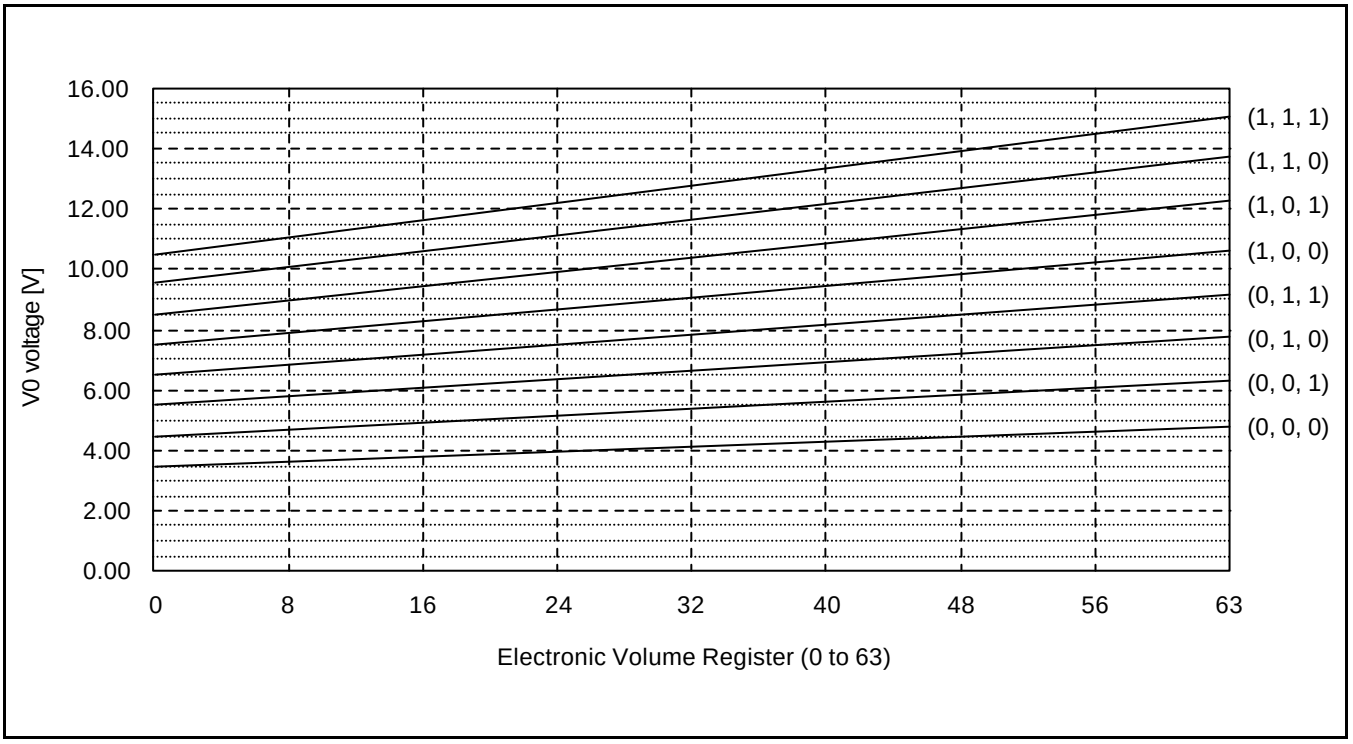

Figure 22. Electronic Volume Level (Temp. Coefficient = -0.125%/°C)

In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and V_{SS}, and Rb between V0 and VR.

Example: For the following requirements
LCD driver voltage, V0 = 10V
6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$10 = (1 + \frac{Rb}{Ra}) \times V_{EV} \text{ [V]} \text{ ------ (Eq.3)}$$

From Eq. 2

$$V_{EV} = (1 - \frac{(63-32)}{210}) \times 2.1 = 1.79 \text{ [V]} \text{ ------ (Eq. 4)}$$

From requirement 3.

$$\frac{10}{Ra + Rb} = 1 \text{ [uA]} \text{ ------ (Eq. 5)}$$

From equations Eq. 3, 4 and 5
Ra = 1.79 [MΩ]
Rb = 8.21 [MΩ]

Table 14 Shows the Range of V0 depending on the above Requirements.

Table 14. The Range of V0

	Electronic volume level				
	0	**.....**	**32**	**.....**	**63**
V0	8.21	.....	10.00	.....	11.73

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and those output impedance are converted by the Voltage Follower for increasing drive capability. Table 15 shows the relationship between V1 to V4 level and each duty ratio.

Table 15. The Relationship between V1 to V4 Level and Each Duty Ratio

LCD bias	V1	V2	V3	V4	Remarks
1/N	(N-1)/N x V0	(N-2)/N x V0	2/N x V0	1/N x V0	N = 5 to 12

REFERENCE CIRCUIT EXAMPLES

[C1 = 1.0 to 4.7 [µF], C2 = 0.47 to 2.0 [µF]]

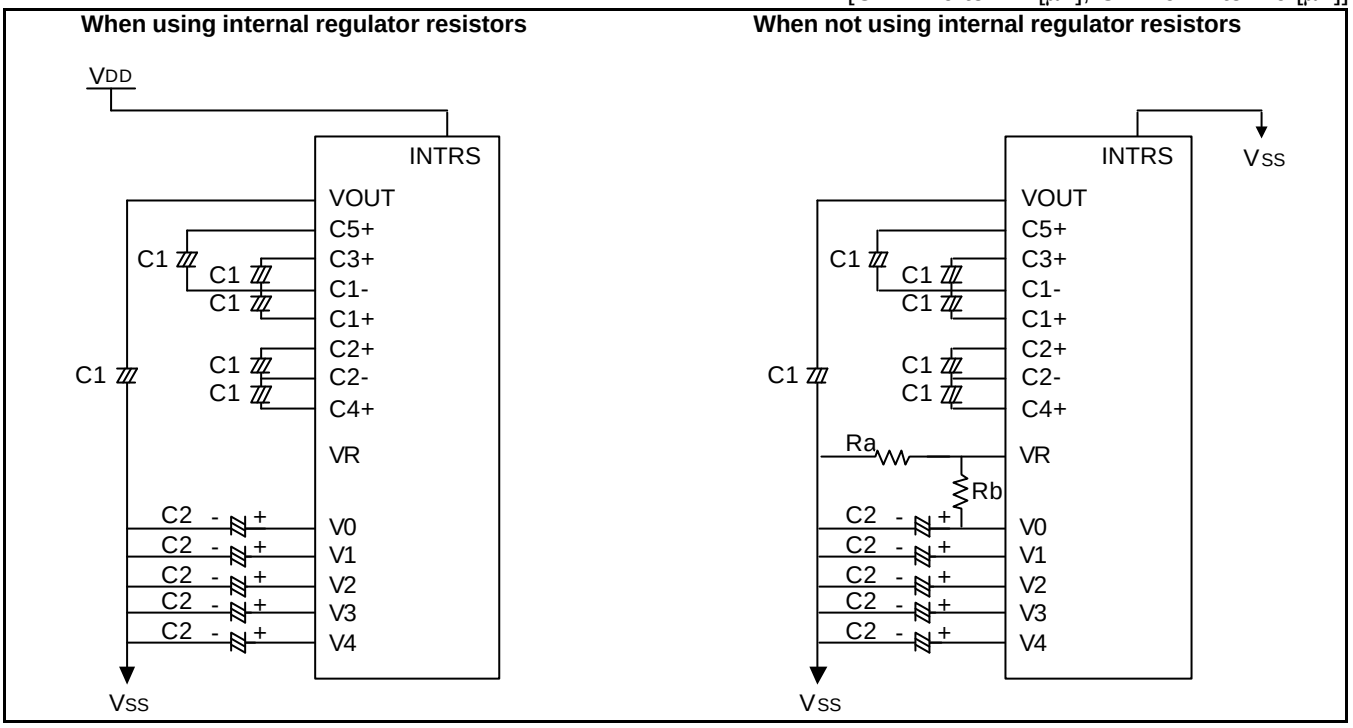

Figure 23. When Using all LCD Power Circuits (6-Time V/C: ON, V/R: ON, V/F: ON)

[C2 = 0.47 to 2.0 [µF]]

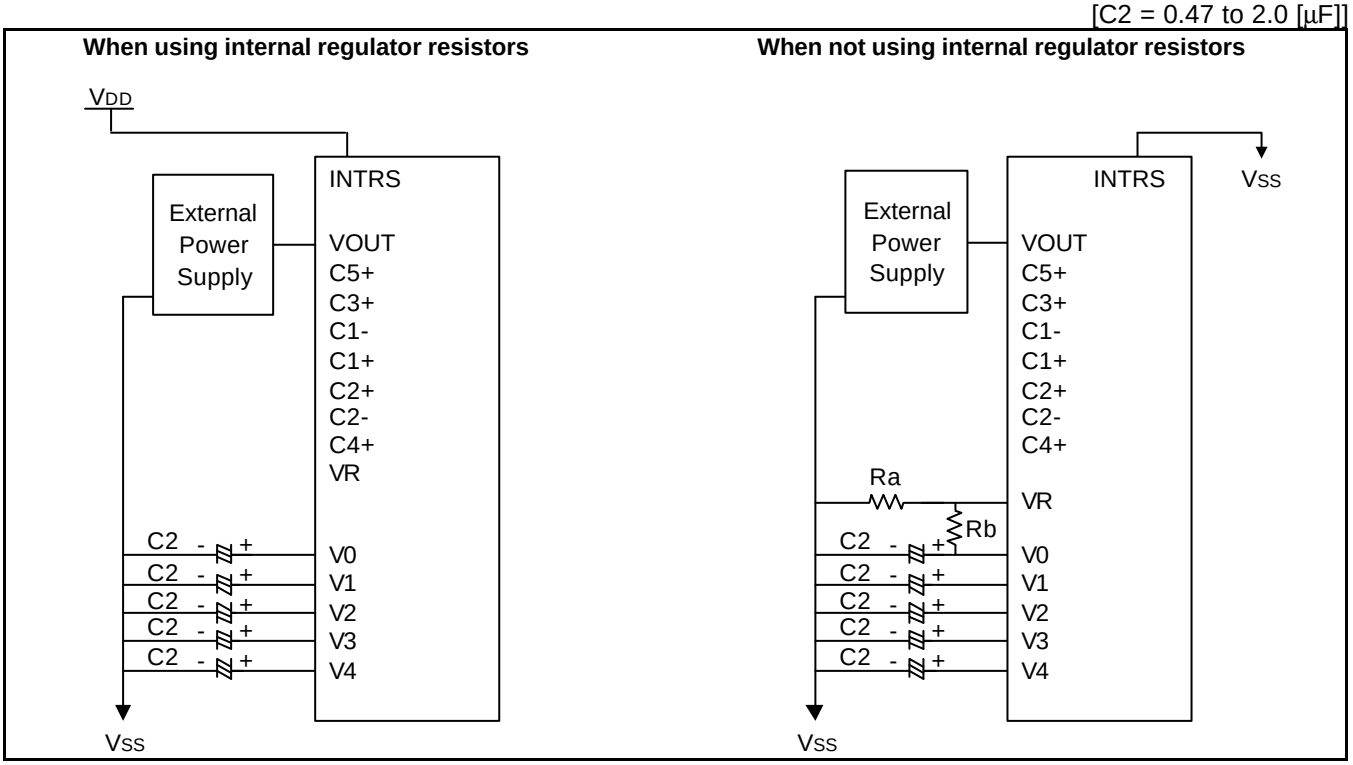

Figure 24. When Using some LCD Power Circuits (V/C: OFF, V/R: ON, V/F: ON)

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[C2 = 0.47 to 2.0 [µF]]

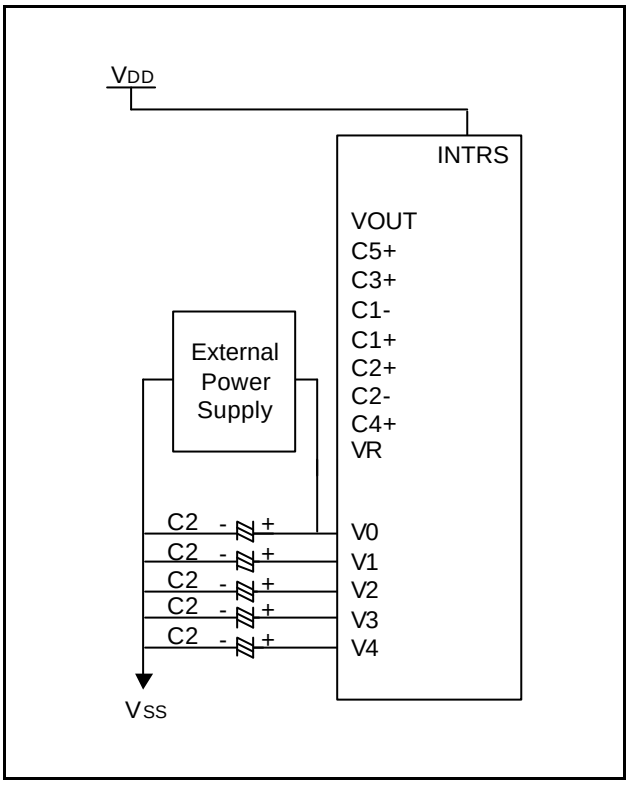

Figure 25. When Using some LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: ON)

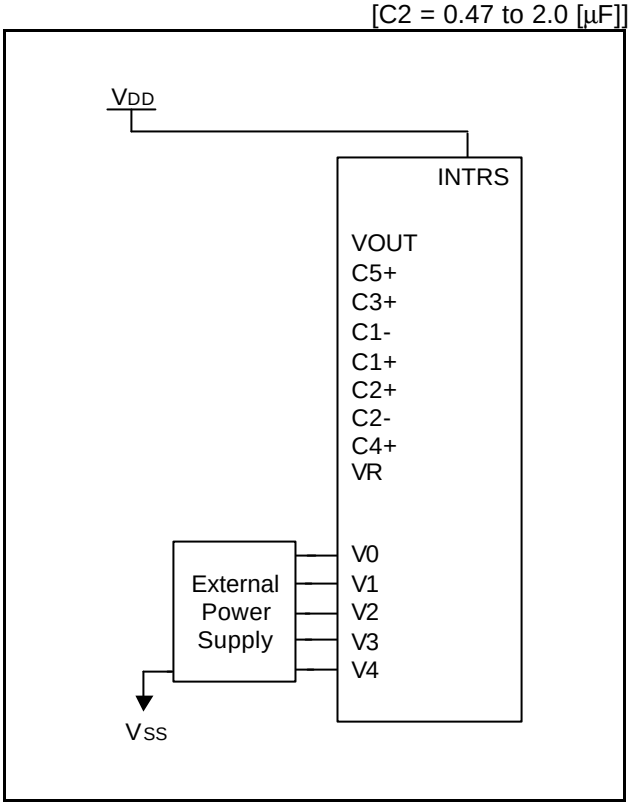

Figure 26. When Not Using any Internal LCD Power Supply Circuits (V/C: OFF, V/R: OFF, V/F: OFF)

RESET CIRCUIT

Setting RESETB to "L" or Reset instruction can initialize internal function.
When RESETB becomes "L", following procedure is occurred.

— Page address: 0
— Column address: 0
— Read-modify-write: OFF
— Display ON/OFF: OFF
— Initial display line: 0 (first)
— Initial COM0 register: 0 (COM0)
— Partial display duty ratio: 1/128
— Reverse display ON/OFF: OFF (normal)
— N-line inversion register: 0 (disable)
— Entire Display ON/OFF: OFF
— ICON Control register ON/OFF: OFF (ICON disable)
— Power control register (VC, VR, VF) = (0, 0, 0)
— DC-DC converter circuit = (0, 0)
— Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
— Contrast Level: 32
— LCD bias ratio: 1/12
— COM Scan Direction: 0
— ADC Select: 0
— Oscillator: OFF
— Power Save Mode: Release
— Display Data Length register: 0 (for SPI mode)
— White mode set: OFF
— White palette register (WG3, WG2, WG1, WG0) = (0, 0, 0, 0)
— Light gray mode set: OFF
— Light gray palette register (LG3, LG2, LG1, LG0) = (0, 0, 0, 0)
— Dark gray mode set: OFF
— Dark gray palette register (DG3, DG2, DG1, DG0) = (1, 1, 1, 1)
— Black mode set: OFF
— Black palette register (BG3, BG2, BG1, BG0) = (1, 1, 1, 1)
— FRC, PWM mode: 4FRC, 9PWM

When RESET instruction is issued, following procedure is occurred.

— Page address: 0
— Column address: 0
— Read-modify-write: OFF
— Initial display line: 0 (First)
— Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
— Contrast Level: 32
— Display Data Length register: 0 (for SPI mode)
— White mode set: OFF
— White palette register (WG3, WG2, WG1, WG0) = (0, 0, 0, 0)
— Light gray mode set: OFF
— Light gray palette register (LG3, LG2, LG1, LG0) = (0, 0, 0, 0)
— Dark gray mode set: OFF
— Dark gray palette register (DG3, DG2, DG1, DG0) = (1, 1, 1, 1)
— Black mode set: OFF
— Black palette register (BG3, BG2, BG1, BG0) = (1, 1, 1, 1)
— FRC, PWM mode: 4FRC, 9PWM

While RESETB is “L” or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes ”L”, any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 16 Instruction Table

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ON/OFF	RES	MF2	MF1	MF0	DS1	DS0	Read the internal status
ICON control register ON/OFF	0	0	1	0	1	0	0	0	1	ICON	ICON=0: ICON disable (default) ICON=1: ICON enable & set the page address to 16
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	0	Y7	Y6	Y5	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y4	Y3	Y2	Y1	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Display ON/OFF	0	0	1	0	1	0	1	1	1	DON	DON=0: display OFF DON=1: display ON
Set initial display line register	0	0	0	1	0	0	0	0	×	×	2-byte instruction to specify the initial display line to realize
	0	0	×	S6	S5	S4	S3	S2	S1	S0	vertical scrolling
Set initial COM0 register	0	0	0	1	0	0	0	1	×	×	2-byte instruction to specify the initial COM0 to realize window
	0	0	×	C6	C5	C4	C3	C2	C1	C0	scrolling
Set partial display duty ratio	0	0	0	1	0	0	1	0	×	×	2-byte instruction to set partial
	0	0	D7	D6	D5	D4	D3	D2	D1	D0	display duty ratio
Set N-line inversion	0	0	0	1	0	0	1	1	×	×	2-byte instruction to set N-line
	0	0	×	×	×	N4	N3	N2	N 1	N0	inversion register
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line Inversion mode
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV	REV=0: normal display, REV=1: reverse display
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	EON=0: normal display. EON=1: entire display ON

NOTE: "×" is don't care.

Table 16. Instruction Table (Continued)

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	0	1	DC1	DC0	Select the step-up of the internal voltage converter
Select regulator resistor	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set electronic volume	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the
register	0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
SHL select	0	0	1	1	0	0	SHL	×	×	×	COM bi-directional selection SHL=0: normal direction SHL=1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-directional selection ADC=0: normal direction ADC=1: reverse direction
Oscillator on start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	P	P=0: normal mode P=1: sleep mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	Release power save mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
Set data direction & display data length(DDL)	×	×	1	1	1	0	1	0	0	0	2-byte instruction to specify the number of data bytes.
	×	×	D7	D6	D5	D4	D3	D2	D1	D0	(SPI Mode)
NOP	0	0	1	1	1	0	0	0	1	1	*No operation*
Test Instruction	0	0	1	1	1	1	×	×	×	×	*Don't use this instruction.*

NOTE: "×" is don't care.

Table 16. Instruction Table (Continued)

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Set FRC and PWM mode	0	0	1	0	0	1	0	FRC	PWM1	PWM0	FRC(1:3FRC, 0:4FRC) PWM1 PWM0 0 0 9PWM 0 1 9PWM 1 0 12PWM 1 1 15PWM
Set white mode and 1st/2nd frame, set	0	0	1	0	0	0	1	0	0	0	Set white mode and 1st/2nd frame
pulse width	0	0	WB3	WB2	WB1	WB0	WA3	WA2	WA1	WA0	
Set white mode and 3rd/4th frame, set	0	0	1	0	0	0	1	0	0	1	Set white mode and 3rd/4th frame
pulse width	0	0	WD3	WD2	WD1	WD0	WC3	WC2	WC1	WC0	
Set light gray mode and 1st/2nd frame, set	0	0	1	0	0	0	1	0	1	0	Set light gray mode and 1st/2nd frame
pulse width	0	0	LB3	LB2	LB1	LB0	LA3	LA2	LA1	LA0	
Set light gray mode and 3rd/4th frame, set	0	0	1	0	0	0	1	0	1	1	Set light gray mode and 3rd/4th frame
pulse width	0	0	LD3	LD2	LD1	LD0	LC3	LC2	LC1	LC0	
Set dark gray mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	1	0	0	Set dark gray mode and 1st/2nd frame
	0	0	DB3	DB2	DB1	DB0	DA3	DA2	DA1	DA0	
Set dark gray mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	1	0	1	Set dark gray mode and 3rd/4th frame
	0	0	DD3	DD2	DD1	DD0	DC3	DC2	DC1	DC0	
Set black mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	1	1	0	Set black mode and 1st/2nd frame
	0	0	BB3	BB2	BB1	BB0	BA3	BA2	BA1	BA0	
Set black mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	1	1	1	Set black mode and 3rd/4th frame
	0	0	BD3	BD2	BD1	BD0	BC3	BC2	BC1	BC0	

Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read Data							

Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write Data							

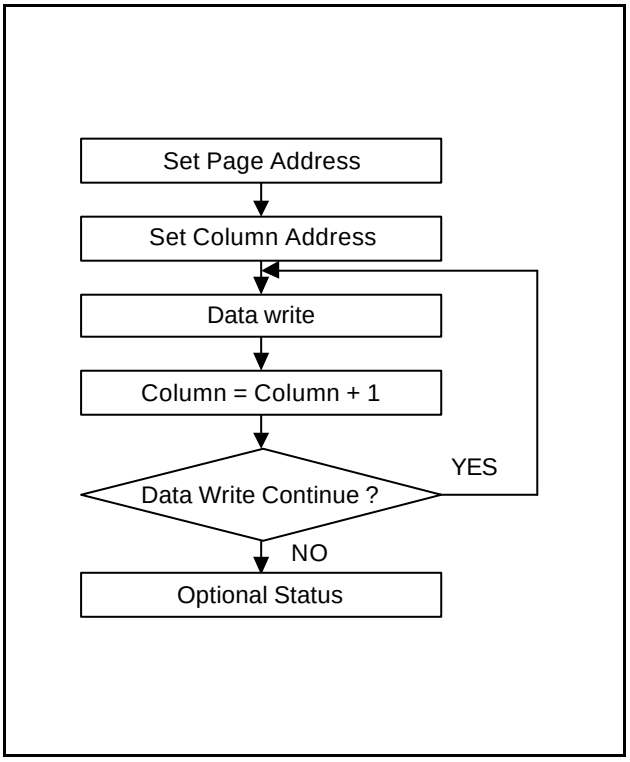

Figure 27. Sequence for Writing Display Data

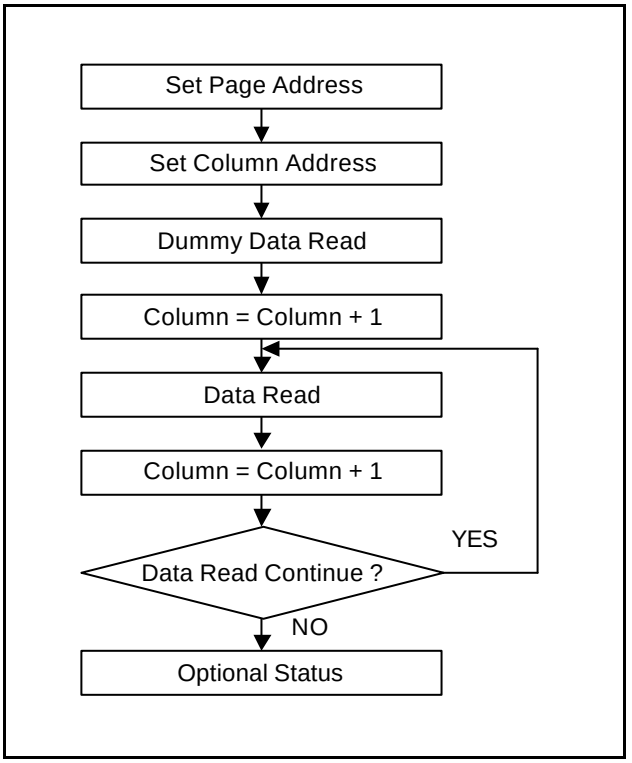

Figure 28. Sequence for Reading Display Data

Read Status

Indicates the internal status of the S6B0741

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ON/OFF	RES	MF2	MF1	MF0	DS1	DS0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy
ON/OFF	Indicates display ON/OFF status 0: display OFF, 1: display ON
RES	Indicates the initialization is in progress by RESET signal. 0: chip is active, 1: chip is being reset
MF	Manufacturer ID, MF2 MF1 MF0 = [0 0 0]
DS	Display size ID, DS1 DS0 = [1 0]

ICON Control Register ON/OFF

This instruction makes ICON enable or disable. By default, ICON display is disabled (ICON= 0). When ICON control register is set to “1”, ICON display is enabled and page address is set to “16”. Then user can write data for icons. It is impossible to set the page address to “16” by Set Page Address instruction. Therefore, when writing data for icons, ICON control register ON instruction would be used to set the page address to “16”. When ICON control register is set to “0”, ICON display is disabled.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	ICON

ICON=0: ICON disable (default)
ICON=1: ICON enable & set the page address to 16

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status. Set Page Address instruction can not be used to set the page address to “16”. Use ICON control register ON/OFF instruction to set the page address to “16”.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y7	Y6	Y5

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y4	Y3	Y2	Y1

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Column address [Y7:Y1]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-Read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-Read mode, and makes the column address return to its initial value just before the set Modify-Read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

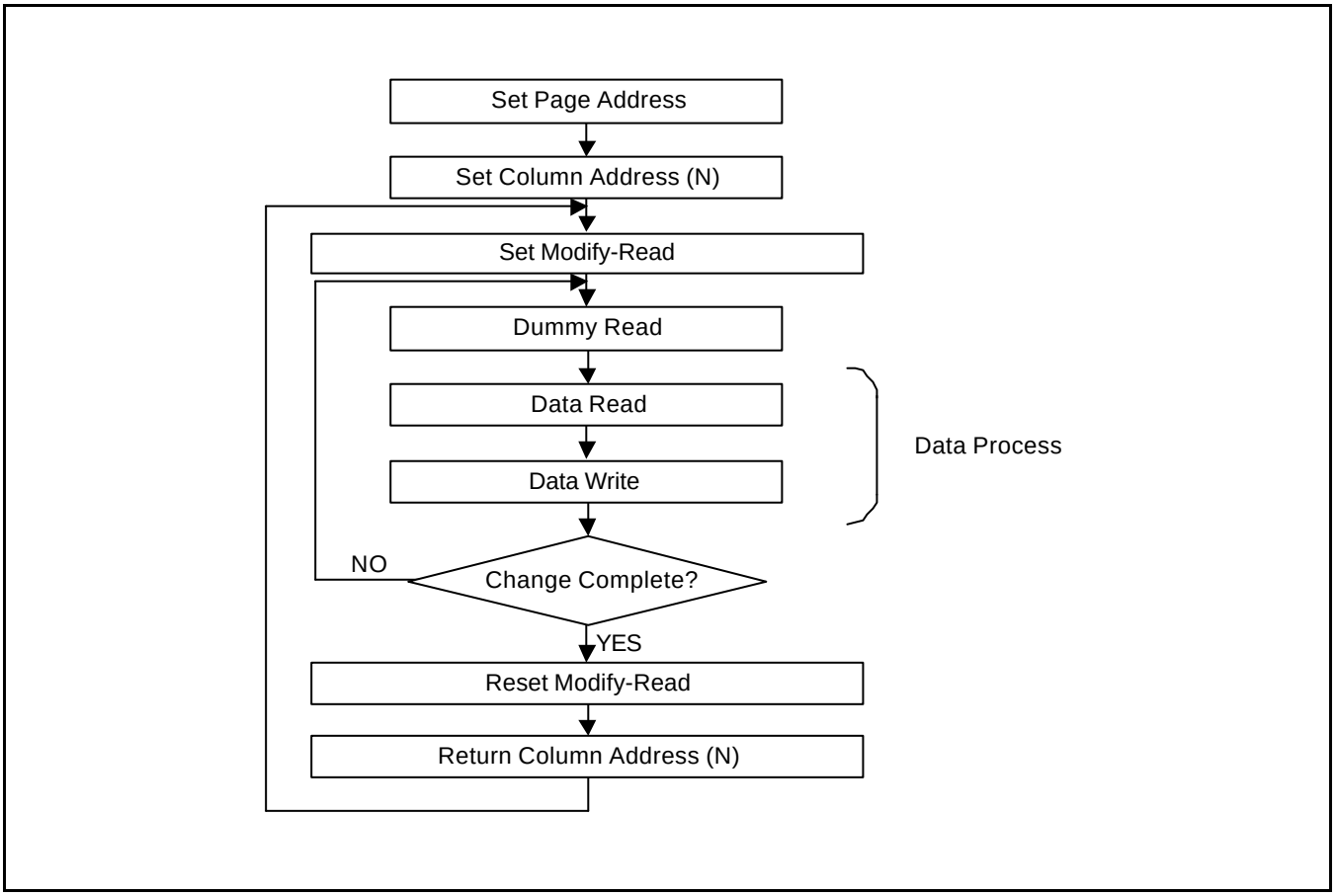

Figure 29. Sequence for Cursor Display

Display ON/OFF

Turns the display ON or OFF.

This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON
DON = 0: display OFF

Set Initial Display Line Register

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top of row(COM0) of LCD panel.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	124
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

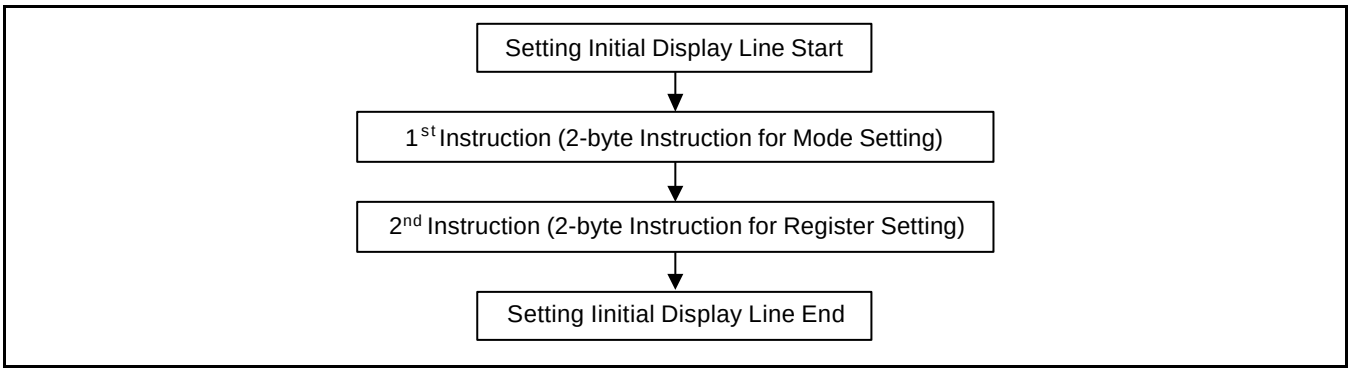

Figure 30. The Sequence for Setting the Initial Display Line

Set Initial COM0 Register

Sets the initial row (COM0) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
0	0	0	0	0	1	1	COM3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	COM124
1	1	1	1	1	0	1	COM125
1	1	1	1	1	1	0	COM126
1	1	1	1	1	1	1	COM127

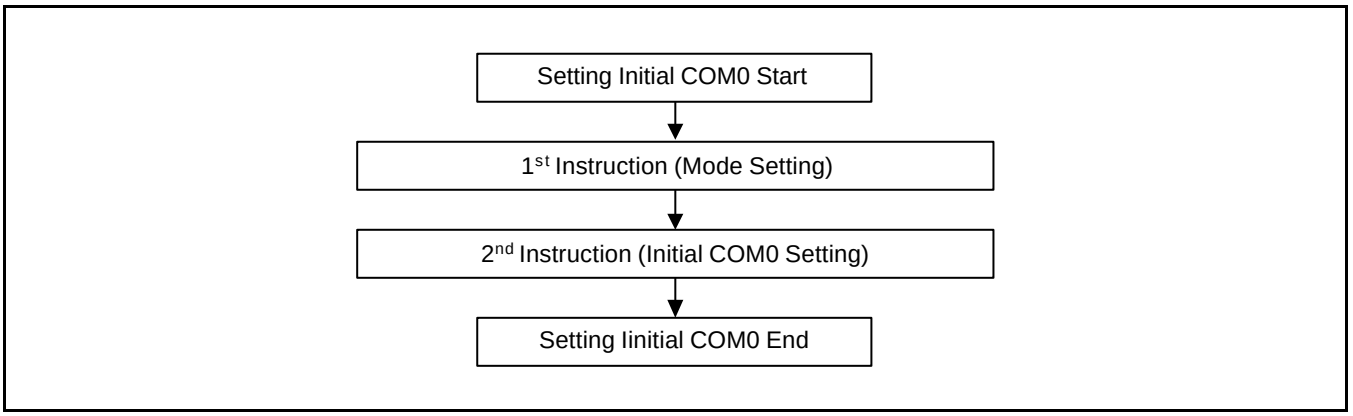

Figure 31. Sequence for Setting the Initial COM0

Set Partial Display Duty Ratio

Sets the duty ratio within range of 16 to 128 (ICON disabled) or 17 to 129 (ICON enabled) to realize partial display by using the 2-byte instruction.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	x	x

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Selected Partial Duty Ratio (ICON Disabled)	Selected Partial Duty Ratio (ICON Enabled)
0	0	0	0	0	0	0	0	No operation	No operation
:	:	:	:	:	:	:	:		
0	0	0	0	1	1	1	1		
0	0	0	1	0	0	0	0	1/16	1/17
0	0	0	1	0	0	0	1	1/17	1/18
:	:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	1/127	1/128
1	0	0	0	0	0	0	0	1/128	1/129
1	0	0	0	0	0	0	1	No operation	No operation
:	:	:	:	:	:	:	:		
1	1	1	1	1	1	1	1		

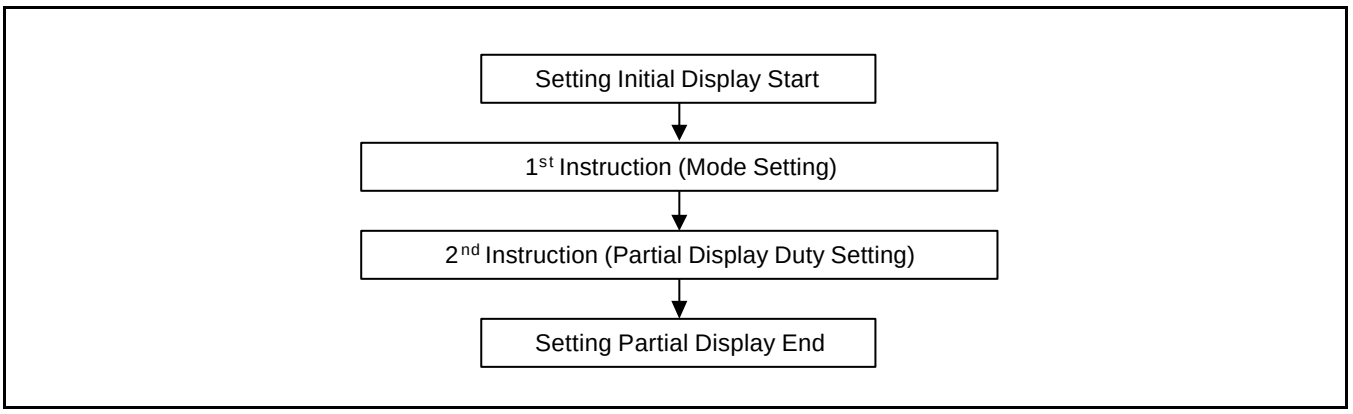

Figure 32. Sequence for Setting Partial Display

Set N-line Inversion Register

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.

The DC-bias problem could be occurred if K is even number. So, we recommend customers to set K to be odd number. K : D/N

D : The number of display duty ratio (D is selectable by customers)

N : N for N-line inversion (N is selectable by customers).

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

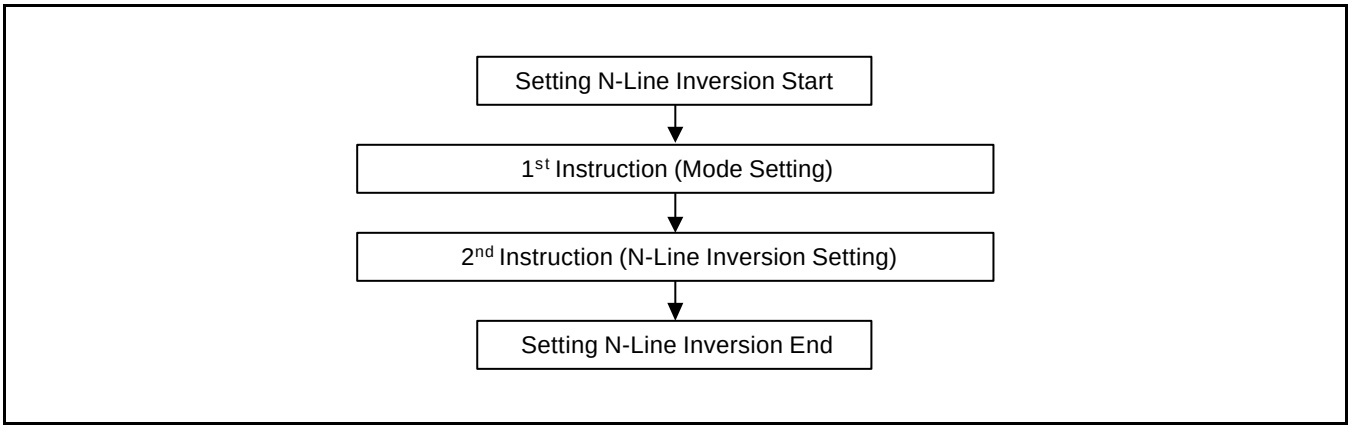

Figure 33. Sequence for N-line Inversion

Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

Reverse Display ON/OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	DDRAM data = "00" – White	DDRAM data = "01" – Light gray	DDRAM data = "10" – Dark gray	DDRAM data = "11" – Dark
0 (normal)	White ("00")	Light gray ("01")	Dark gray ("10")	Dark ("11")
1 (reverse)	Dark ("11")	Dark gray ("10")	Light gray ("01")	White ("00")

Entire Display ON/OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display ON/OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON	DDRAM data = "00" – White	DDRAM data = "01" – Light gray	DDRAM data = "10" – Dark gray	DDRAM data = "11" – Dark
0 (normal)	White ("00")	Light gray ("01")	Dark gray ("10")	Dark ("11")
1 (entire)	Dark ("11")	Dark gray ("11")	Light gray ("11")	White ("11")

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF. Internal voltage converter circuit is ON.
	0 1		Internal voltage regulator circuit is OFF. Internal voltage regulator circuit is ON.
		0 1	Internal voltage follower circuit is OFF. Internal voltage follower circuit is ON.

Select DC-DC Step-up

Selects one of 4 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	1	DC1	DC0

DC1	DC0	Selected DC-DC converter circuit
0	0	3 times boosting circuit
0	1	4 times boosting circuit
1	0	5 times boosting circuit
1	1	6 times boosting circuit

Select Regulator Resistor

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1+ (Rb/Ra)
0	0	0	2.3
0	0	1	3.0
0	1	0	3.7
0	1	1	4.4
1	0	0	5.1
1	0	1	5.8
1	1	0	6.5
1	1	1	7.2

Set Electronic Volume Register

Consist of 2-byte Instructions
The 1st instruction set Reference Voltage mode, the 2nd one updates the contents of reference voltage register.
After second instruction, Reference Voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

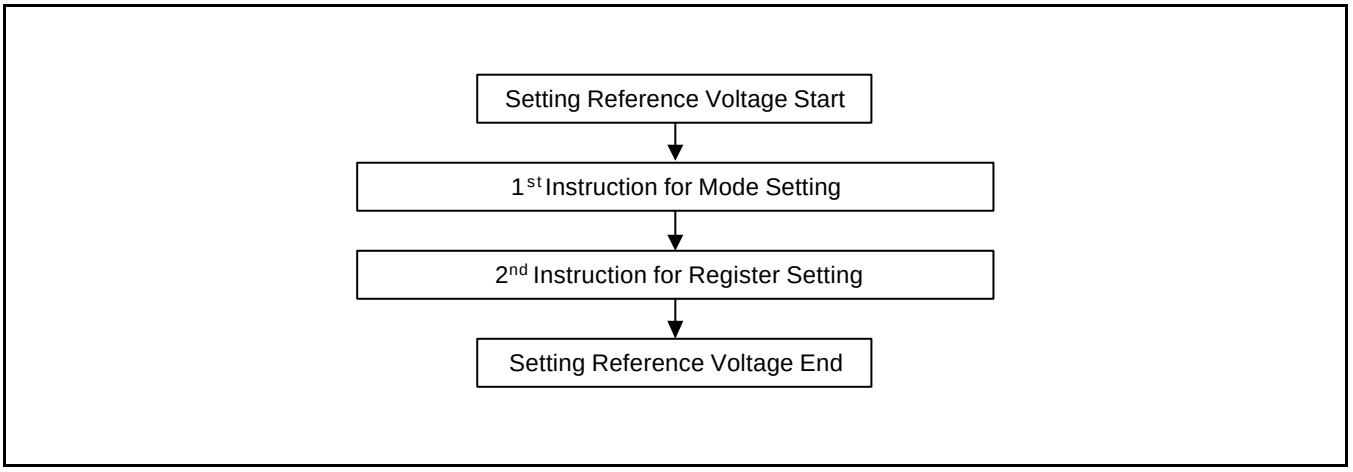

Figure 34. Sequence for Setting the Electronic Volume

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	LCD bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

× : Don' t care

SHL = 0: normal direction (COM0 → COM127)
SHL = 1: reverse direction (COM127 → COM0)

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG127)
ADC = 1: reverse direction (SEG127 → SEG0)

Oscillator ON Start

This instruction enables the built-in oscillator circuit.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

Power Save

The S6B0741 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = 0: normal mode
P = 1: sleep mode

Release Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

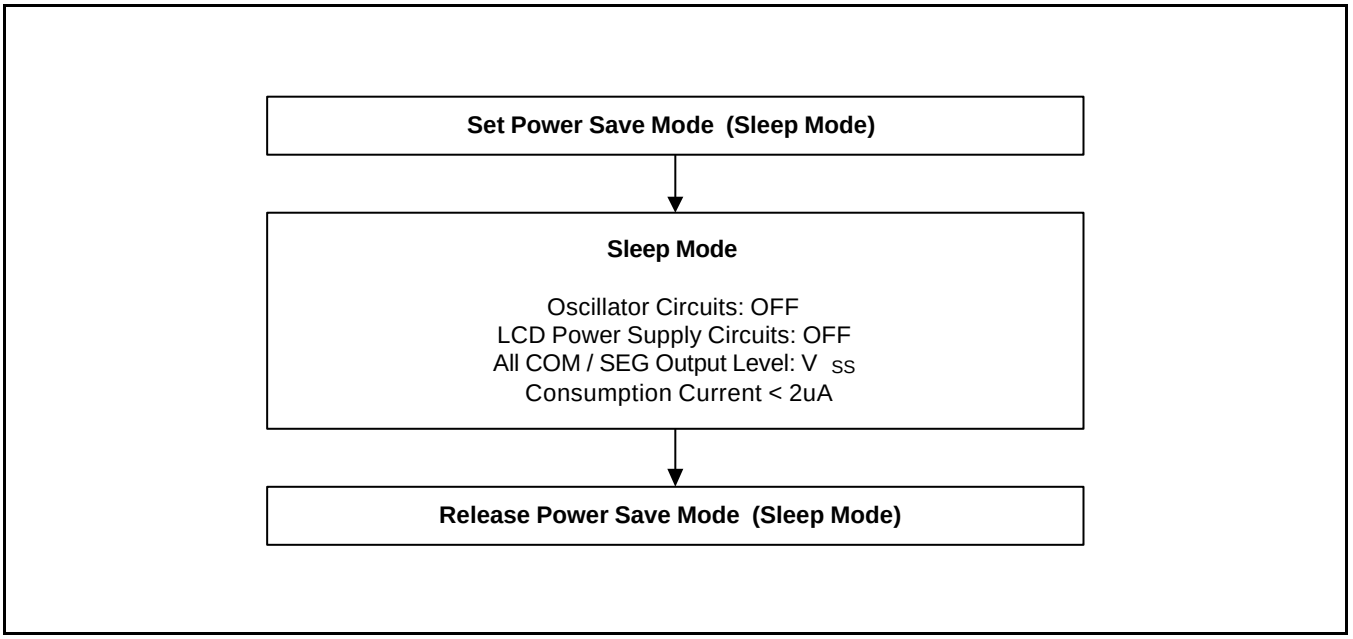

Figure 35. Power Save Routine

Reset

This instruction Resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

Set Data Direction & Display Data Length (3-Pin SPI Mode)

Consists of 2 bytes instruction.
This command is used in 3-Pin SPI mode only(PS0 = "L" and PS1 = "L"). It will be two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When RS is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command data.

The 1st Instruction: Set Data Direction (Only Write Mode)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	1	1	1	0	1	0	0	0

The 2nd Instruction: Set Display Data Length (DDL) Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

NOP

No operations

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test Instruction

This instruction is for testing IC. Please do not use it.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	×	×	×	×

Set PWM & FRC mode

Selects 3/4 FRC and 9/12/15 PWM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	FRC	PWM1	PWM0

FRC	PWM1	PWM0	Status of PWM & FRC
0			4FRC
1			3FRC
	0	0	9PWM
	0	1	9PWM
	1	0	12PWM
	1	1	15PWM

Set Gray Scale Mode & Register

Consists of 2 bytes instruction. The first byte sets grayscale mode and the second byte updates the contents of gray scale register without issuing any other instruction.

Set Gray Scale Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	GM2	GM1	GM0

GM2	GM1	GM0	Description
0	0	0	In case of setting white mode and 1st/2nd frame.
0	0	1	In case of setting white mode and 3rd/4th frame.
0	1	0	In case of setting light gray mode and 1st/2nd frame.
0	1	1	In case of setting light gray mode and 3rd/4th frame.
1	0	0	In case of setting dark gray mode and 1st/2nd frame.
1	0	1	In case of setting dark gray mode and 3rd/4th frame.
1	1	0	In case of setting black mode and 1st/2nd frame.
1	1	1	In case of setting black mode and 3rd/4th frame.

Set Gray Scale Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	GB3	GB2	GB1	GB0	GA3	GA2	GA1	GA0
0	0	GD3	GD2	GD1	GD0	GC3	GC2	GC1	GC0

GA3, GB3, GC3, GD3	GA2, GB2, GC2, GD2	GA1, GB1, GC1, GD1	GA0, GB0, GC0, GD0	Pulse width (9PWM)	Pulse width (12PWM)	Pulse width (15PWM)
0	0	0	0	0/9	0/12	0/15
0	0	0	1	1/9	1/12	1/15
:	:	:	:	:	:	:
1	0	0	1	9/9	9/12	9/15
1	0	1	0	0/9	10/12	10/15
1	0	1	1	0/9	11/12	11/15
1	1	0	0	0/9	12/12	12/15
1	1	0	1	0/9	0/12	13/15
1	1	1	0	0/9	0/12	14/15
1	1	1	1	0/9	0/12	15/15

NOTE: GA3=WA3,LA3,DA3,BA3 GA2=WA2,LA2,DA2,BA2 GA1=WA1,LA1,DA1,BA1 GA0=WA0,LA0,DA0,BA0
GB3=WB3,LB3,DB3,BB3 GA2=WB2,LB2,DB2,BB2 GA1=WB1,LB1,DB1,BB1 GA0=WB0,LB0,DB0,BB0
GC3=WC3,LC3,DC3,BC3 GA2=WC2,LC2,DC2,BC2 GA1=WC1,LC1,DC1,BC1 GA0=WC0,LC0,DC0,BC0
GD3=WD3,LD3,DD3,BD3 GA2=WD2,LD2,DD2,BD2 GA1=WD1,LD1,DD1,BD1 GA0=WD0,LD0,DD0,BD0

Referential Instruction Set-up Flow: Initializing with the built-in Power Supply Circuits

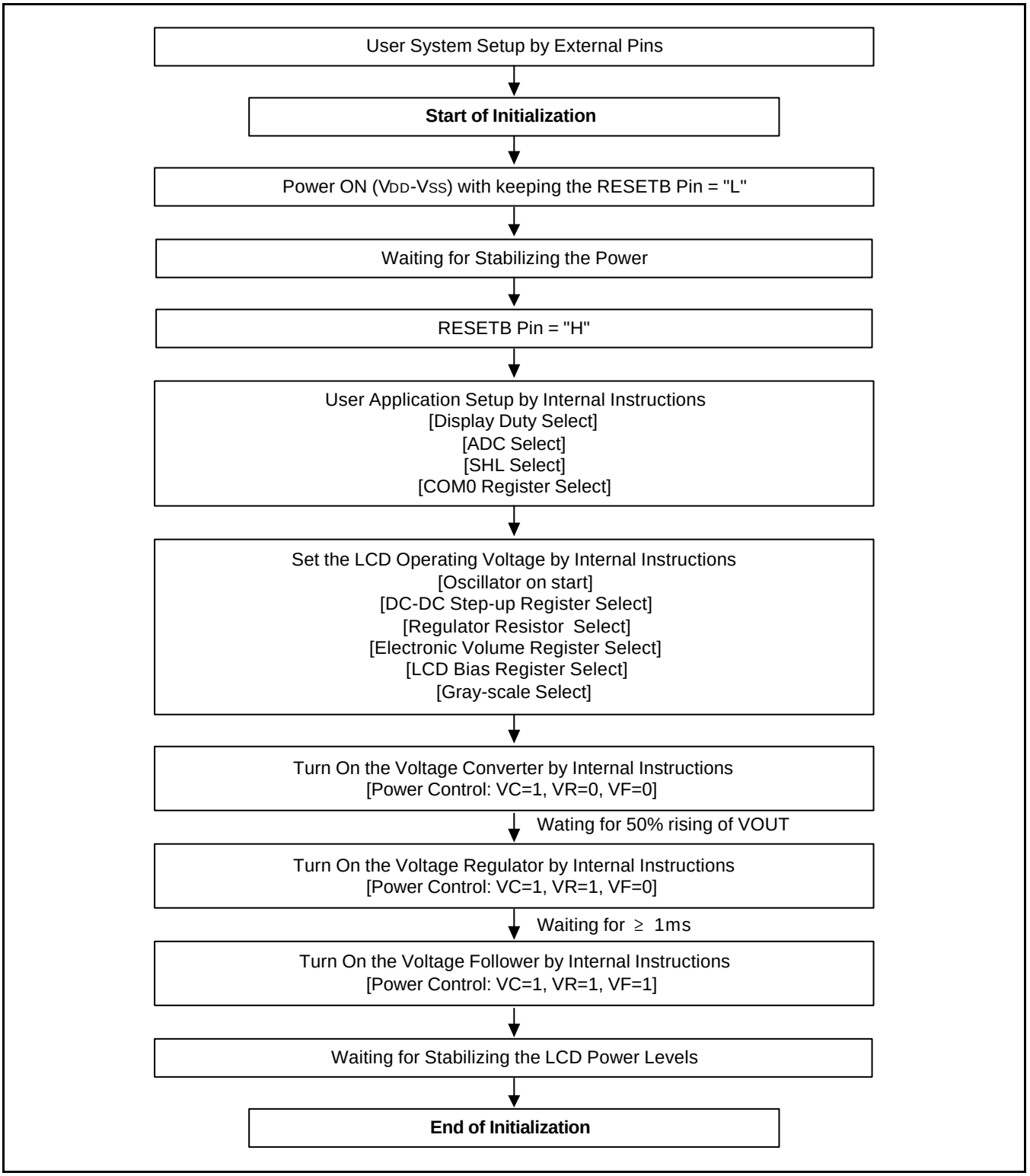

Figure 36. Initializing with the Built-in Power Supply Circuits

Referential Instruction Set-up Flow: Initializing without the built-in Power Supply Circuits

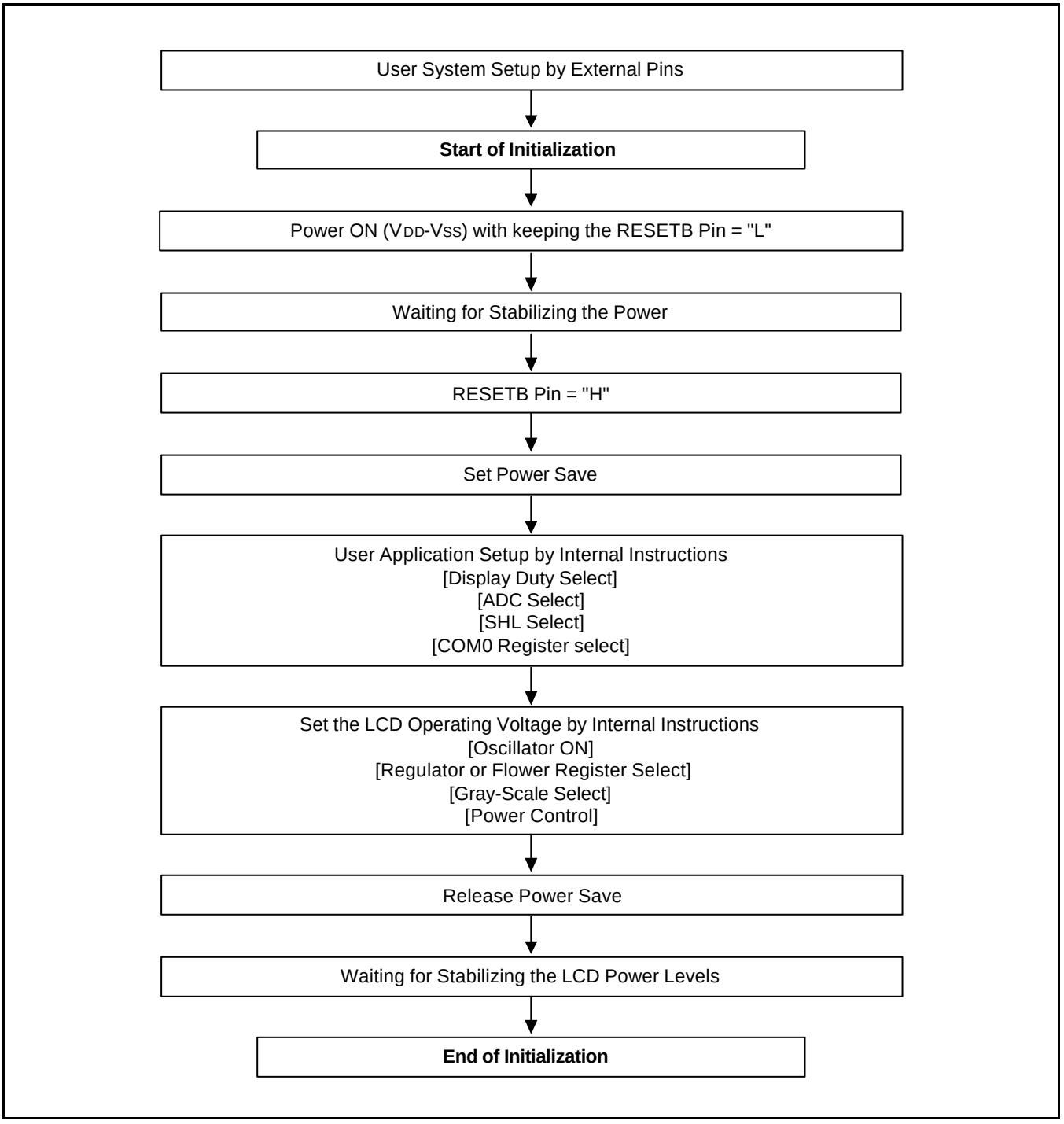

Figure 37. Initializing without the Built-in Power Supply Circuits

Referential Instruction Set-up Flow: Data Displaying

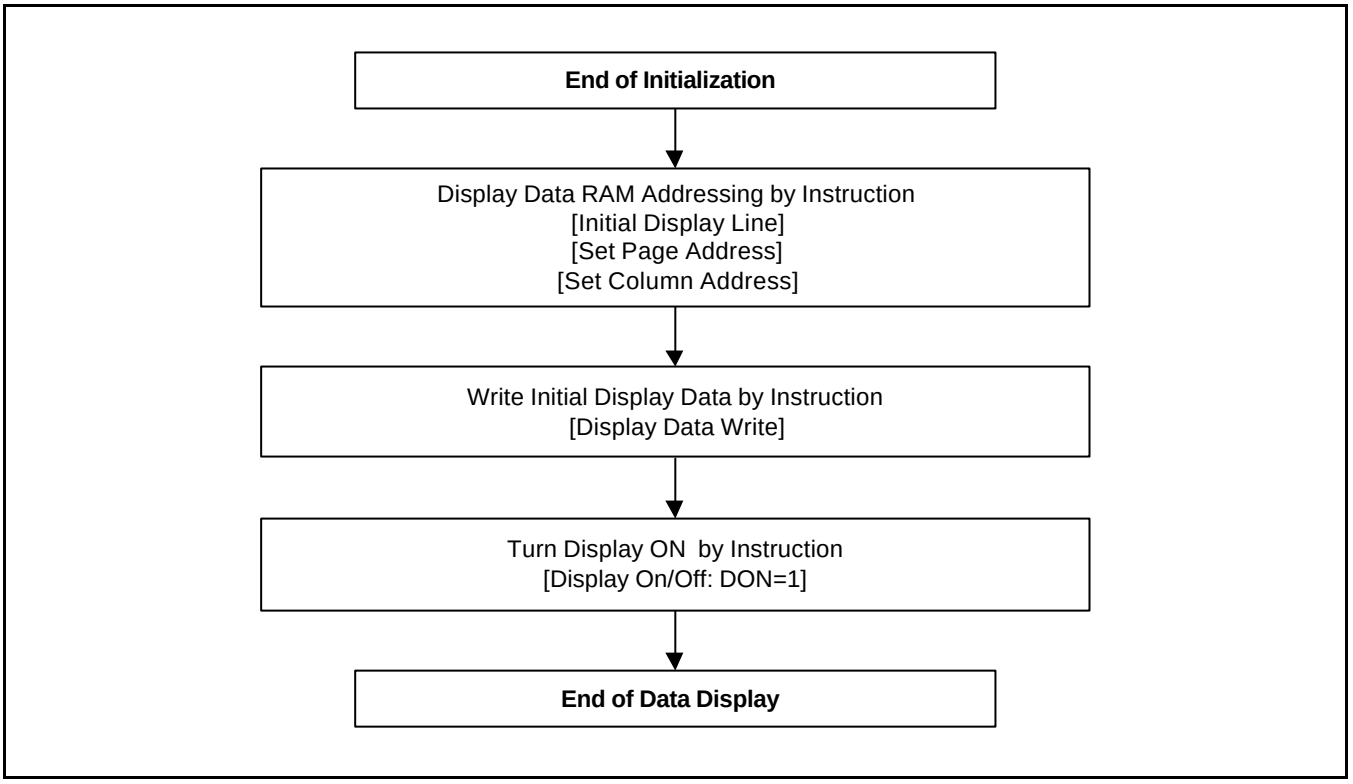

Figure 38. Data Displaying

Referential Instruction Set-up Flow: Power OFF

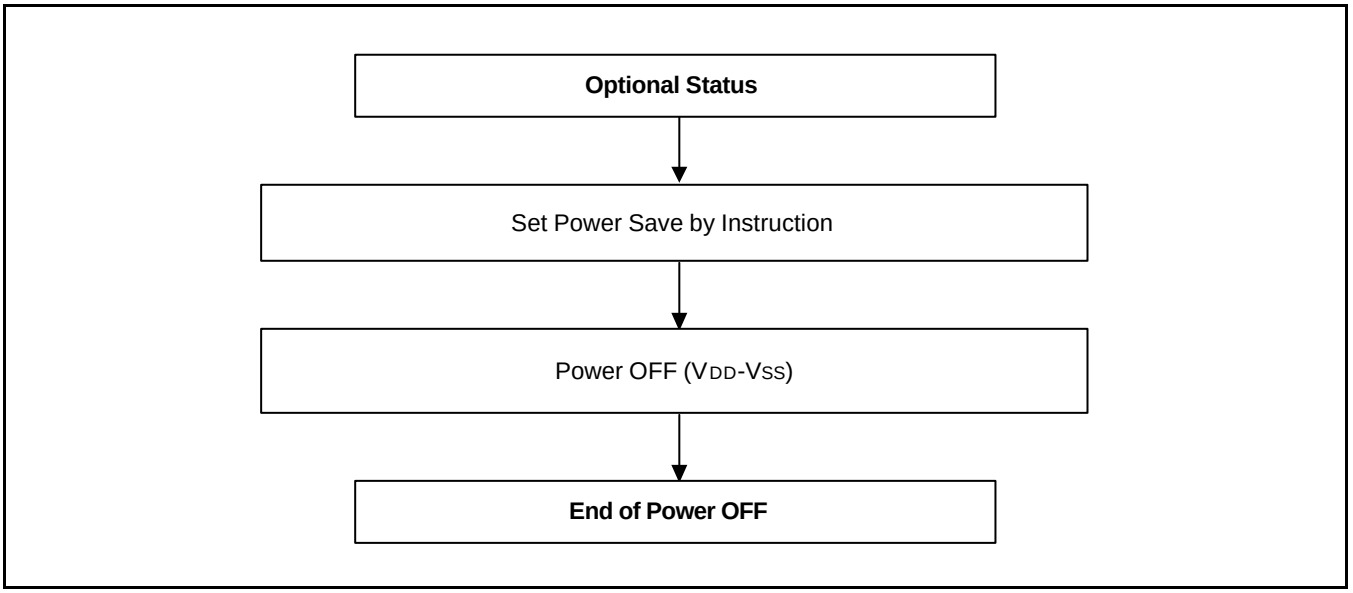

Figure 39. Power OFF

Referential Instruction Set-up Flow: Partial Duty Changing

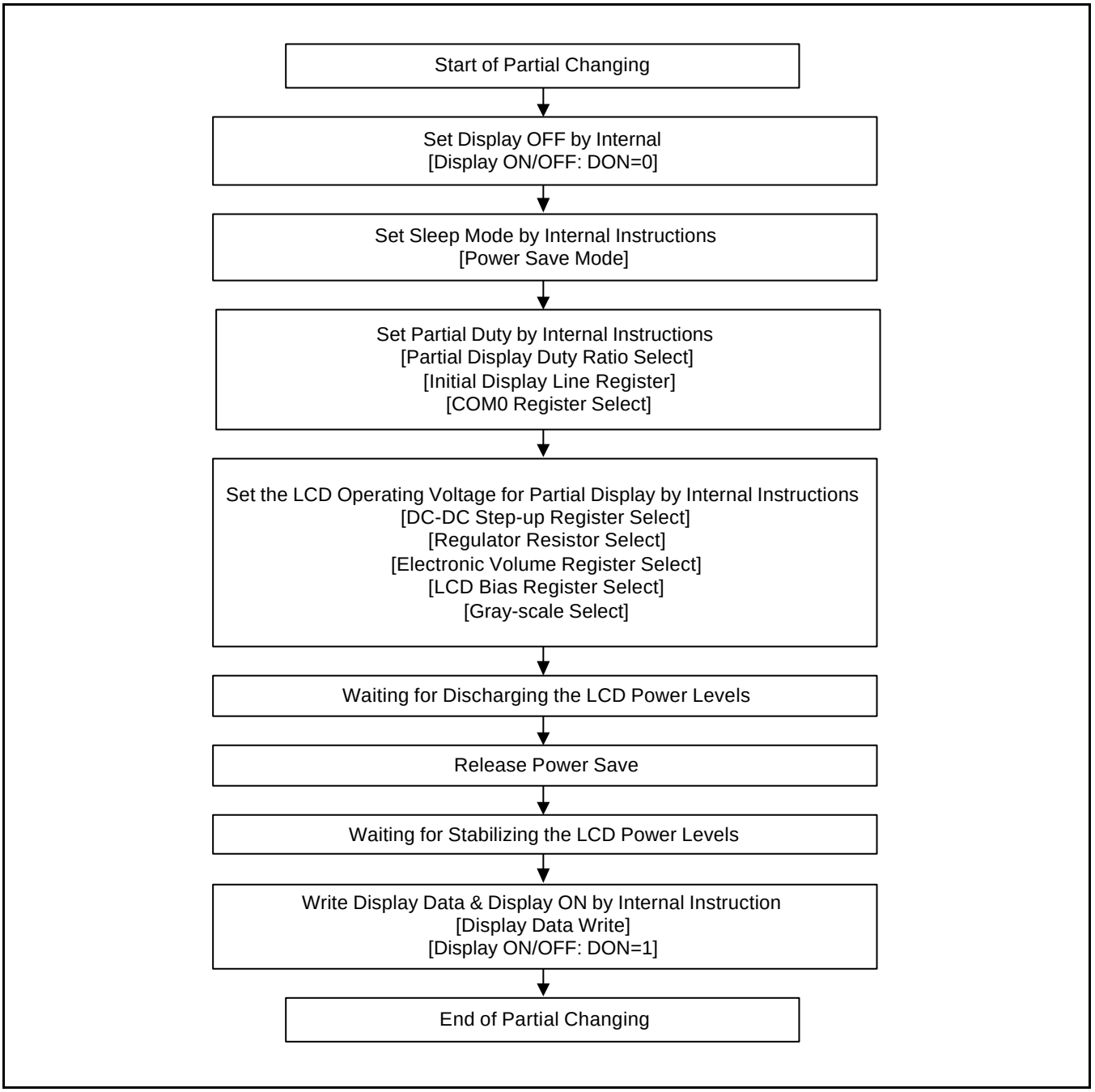

Figure 40. Partial Duty Changing

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 17. Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	- 0.3 to + 7.0	V
	V0, VOUT	- 0.3 to + 17.0	V
	V1, V2, V3, V4	- 0.3 to V0 + 0.3	V
External reference voltage	VEXT	+0.3 to V_{DD}	V
Input voltage range	V_{IN}	- 0.3 to V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	- 40 to + 85	°C
Storage temperature range	T_{STR}	- 55 to + 125	°C

NOTES:

1. V_{DD}, V0, VOUT, V1 to V4 and VEXT are based on VSS = 0V.
2. Voltages $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V_{SS}$ must always be satisfied.($V_{LCD} = V0 - V_{SS}$)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 18. DC Characteristics

(V_{SS} = 0V, V_{DD} = 1.8 to 3.3V, Ta = -40 to 85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating Voltage (1)		V_{DD}		1.8	-	3.3	V	V_{DD} (1)
Operating Voltage (2)		V0		4.0	-	15.0	V	V0 (2)
Input Voltage	High	V_{IH}		$0.8V_{DD}$	-	V_{DD}	V	(3)
	Low	V_{IL}		V_{SS}	-	$0.2V_{DD}$		
Output Voltage	High	V_{OH}	I_{OH} = -0.5mA	$0.8V_{DD}$	-	V_{DD}	V	(4)
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	$0.2V_{DD}$		
Input Leakage Current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	(3)
Output Leakage Current		I_{OZ}	VIN = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	(5)
LCD Driver ON Resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn (6)
Operating Frequency		f_{FR}	Ta = 25°C 1/128 Duty, 9 PWM REXT = 620kΩ (*11)	70	85	100	Hz	(7), (11)
Voltage Converter Input Voltage		V_{CI}	× 3	1.8	-	3.6	V	VCI
			× 4	1.8	-	3.6		
			× 5	1.8	-	3.0		
			× 6	1.8	-	2.5		
Voltage Converter Output Voltage		V_{OUT}	x3/×4/×5/×6 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage Regulator Operating Voltage		V_{OUT}		5.4	-	15.0	V	VOUT
Voltage Follower Operating Voltage		V0		4.0	-	15.0	V	V0 (8)
Reference Voltage		V_{REF}	Ta = 25°C	2.04	2.10	2.16	V	(9)

Dynamic Current Consumption when The Internal Power Supply is ON

Table 19. Dynamic Current 2 (Internal Power)

(V_{DD} = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic Current Consumption	I_{DD}	V0 - V_{SS} = 12.0V, x5 boosting, duty = 1/128, normal mode (Display Off)	-	100	150	µA	(10)
		V0 - V_{SS} = 12.0V, x5 boosting, duty = 1/128, normal mode (Display On , Checker Pattern)	-	200	300	µA	(10)

Current Consumption during Power Save Mode

Table 20. Power Save Mode Current

(V_{DD} = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep Mode Current	I_{DDS1}	During Sleep	-	-	2	µA	(10)

Table 21. The Relationship between Oscillation Frequency and Frame Frequency

Duty ratio	Item	f_{CL}	f_{OSC}
1/N	On-chip oscillator circuit is used	f_{FR} x N	f_{FR} x PWM x 2 x N

(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: frame frequency, N = 16 to 129)

NOTES:

1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
2. In case of external power supply is applied.
3. CSB, RS, DB0 to DB7, E_RD, RW_WR, RESETB, PS1, PS0, INTRS and REF
4. DB0 to DB7
5. Applies when the DB0 to DB7 pins are in high impedance.
6. Resistance value when -0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
   RON [kΩ] = ΔV[V]/0.1[mA] (ΔV : voltage change when -0.1[mA] is applied in the ON status.)
7. See Table 22 for the relationship between oscillation frequency and frame frequency.
8. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
9. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
10. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
    The current consumption, when the built-in power supply circuit is ON.
    The current flowing through voltage regulation resistors(Rb and Ra) is not included.
    It does not include the current of the LCD panel capacity, wiring capacity, etc.
    Other conditions are 1/12 bias, 3 FRC, 9 PWM, Frame inversion, Frame freq. = 85HZ, BL=(9,9,9,0), DG=(6,6,6,0), LG=(3,3,3,0), WH=(0,0,0,0).
11. Applies when PWM method is used.
    When both PWM and FRC method are used, frame frequency should be increased up to more than 130Hz. So, oscillator resistor value between OSC1 and V_{DD} pin should be reduced.

AC CHARACTERISTICS

Read/Write Characteristics (8080-series MPU)

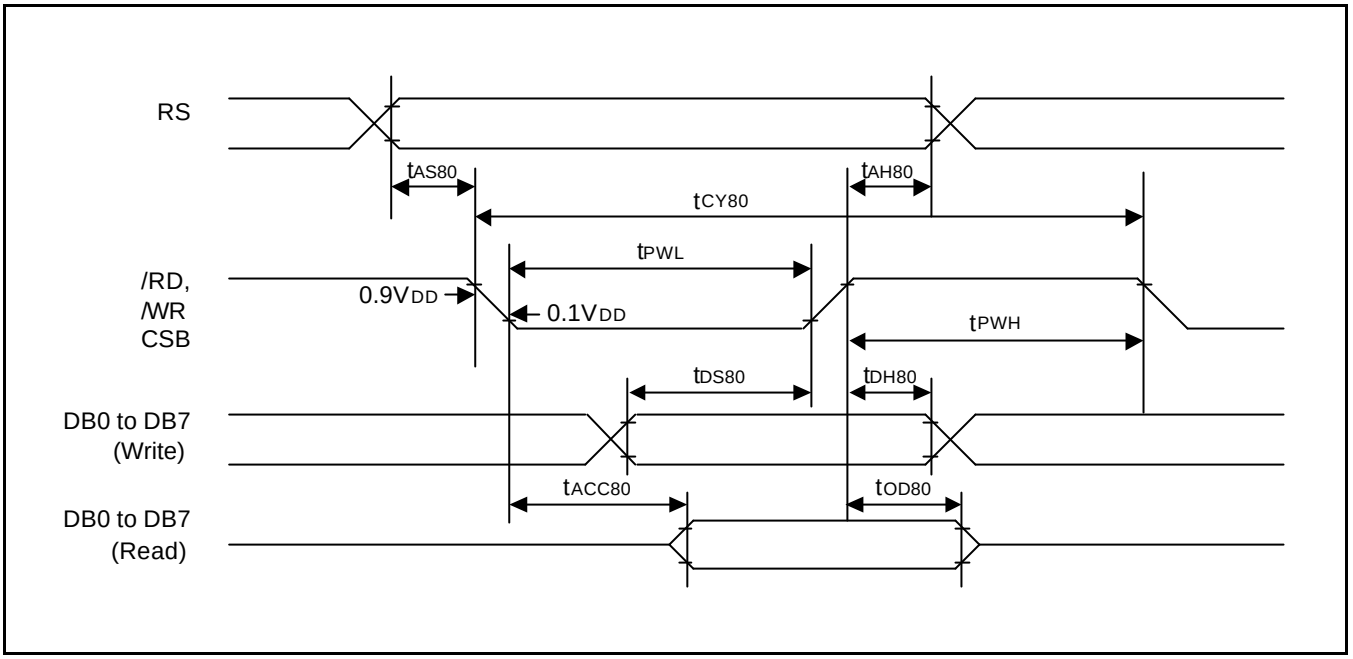

Figure 41. Read/Write Characteristics (8080-series MPU)

(V_{DD} = 1.8V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address Setup Time Address Hold Time	RS	t_{AS80} t_{AH80}		0 0	- -	ns
System Cycle Time For Write System Cycle Time For Read		t_{CY80} t_{CY80}		150 330	-	ns
Pulse Width Low Pulse Width High	/WR /RD	t_{PWL} t_{PWH}		60 60	- -	ns
Data Setup Time Data Hold Time	DB0-DB7	t_{DS80} t_{DH80}		40 10	- -	ns
Read Access Time Output Disable Time		t_{ACC80} t_{OD80}	CL = 100 pF	15 10	- 50	ns

(V_{DD} = 2.7V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address Setup Time Address Hold Time	RS	t_{AS80} t_{AH80}		0 0	- -	ns
System Cycle Time For Write System Cycle Time For Read		t_{CY80} t_{CY80}		100 166	-	ns
Pulse Width Low Pulse Width High	/WR /RD	t_{PWL} t_{PWH}		40 40	- -	ns
Data Setup Time Data Hold Time	DB0-DB7	t_{DS80} t_{DH80}		30 5	- -	ns
Read Access Time Output Disable Time		t_{ACC80} t_{OD80}	CL = 100 pF	15 10	- 50	ns

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (t_{CY80} - t_{PWLW} - t_{PWHW}) for write, (tr + tf) < (t_{CY80} - t_{PWLR} - t_{PWHR}) for read.

Read/Write Characteristics (6800-series Microprocessor)

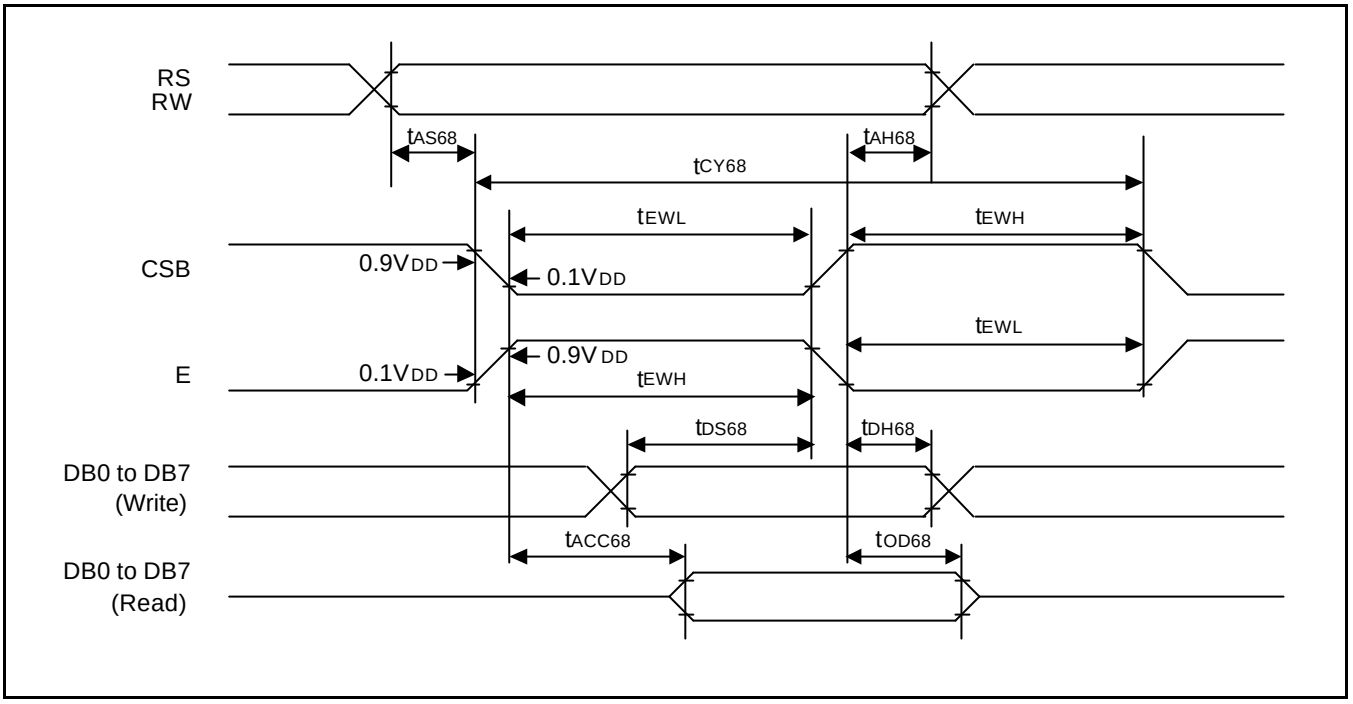

Figure 42. Read/Write Characteristics (6800-series Microprocessor)

(V_{DD} = 1.8V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address Setup Time Address Hold Time	RS RW_WR	t_{AS68} t_{AH68}		0 0	- -	ns
System Cycle Time For Write System Cycle Time For Read		t_{CY68} t_{CY68}		150 330	-	ns
Enable Width High Enable Width Low	E_RD (E)	t_{EWH} t_{EWL}		60 60	- -	ns
Data Setup Time Data Hold Time	DB0 to DB7	t_{DS68} t_{DH68}		40 10	- -	ns
Read Access Time Output Disable Time		t_{ACC68} t_{OD68}	C_L = 100 pF	15 10	- 50	ns

(V_{DD} = 2.7V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address Setup Time Address Hold Time	RS RW_WR	t_{AS68} t_{AH68}		0 0	- -	ns
System Cycle Time For Write System Cycle Time For Read		t_{CY68} t_{CY68}		100 166	-	ns
Enable Width High Enable Width Low	E_RD (E)	t_{EWH} t_{EWL}		40 40	- -	ns
Data Setup Time Data Hold Time	DB0- DB7	t_{DS68} t_{DH68}		30 5	- -	ns
Read Access Time Output Disable Time		t_{ACC68} t_{OD68}	C_L = 100 pF	15 10	- 50	ns

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
$(tr + tf) < (t_{CY68} - t_{EWHW} - t_{EWLW})$ for write, $(tr + tf) < (t_{CY68} - t_{EWHR} - t_{EWLR})$ for read.

Serial Interface Characteristics

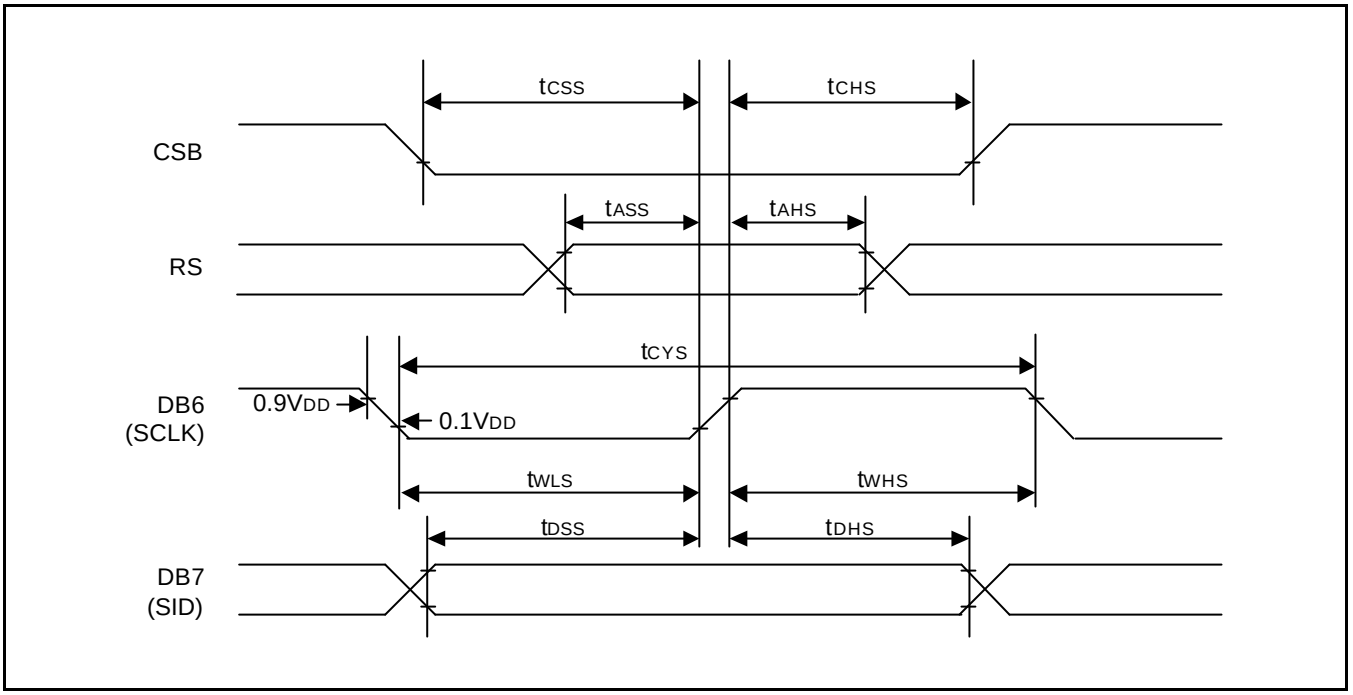

Figure 43. Serial Interface Characteristics

(V_{DD} = 1.8V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial Clock Cycle SCLK High Pulse Width SCLK Low Pulse Width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}		111 60 60	- - -	ns
Address Setup Time Address Hold Time	RS	t_{ASS} t_{AHS}		60 60	- -	ns
Data Setup Time Data Hold Time	DB7 (SID)	t_{DSS} t_{DHS}		60 60	- -	ns
CSB Setup Time CSB Hold Time	CSB	t_{CSS} t_{CHS}		60 1/2 * t_{CYS}	- -	ns

(V_{DD} = 2.7V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial Clock Cycle SCLK High Pulse Width SCLK Low Pulse Width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}		58.8 30 30	- - -	ns
Address Setup Time Address Hold Time	RS	t_{ASS} t_{AHS}		30 30	- -	ns
Data Setup Time Data Hold Time	DB7 (SID)	t_{DSS} t_{DHS}		30 30	- -	ns
CSB Setup Time CSB Hold Time	CSB	t_{CSS} t_{CHS}		30 1/2 * t_{CYS}	- -	ns

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Reset Input Timing

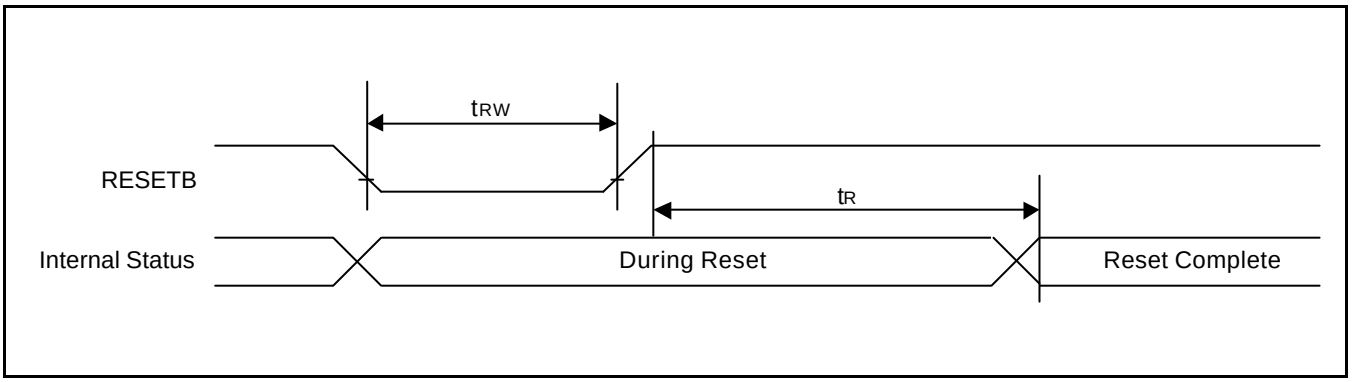

Figure 44. Reset Input Timing

(V_{DD} = 1.8 to 3.3V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset Low Pulse Width	RESETB	t_{RW}		1000	-	ns
Reset Time	-	t_R		-	1000	ns

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS0 = "H", PS1 = "H")

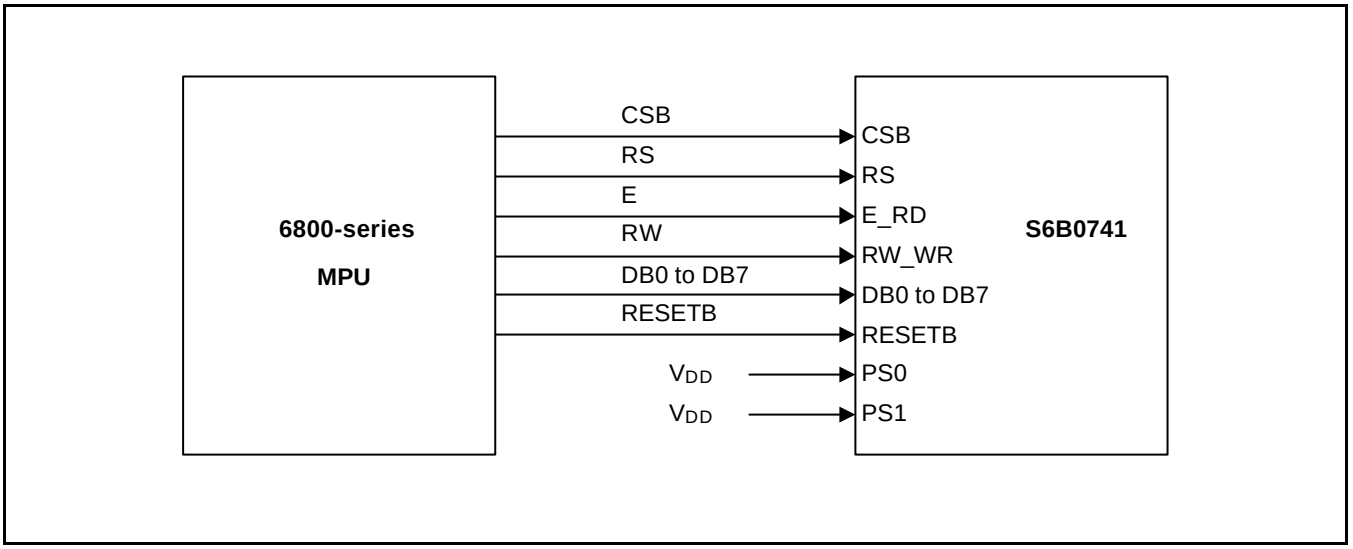

Figure 45. Interfacing with 6800-series (PS0 = "H", PS1 = "H")

In Case of Interfacing with 8080-series (PS0 = "H", PS1 = "L")

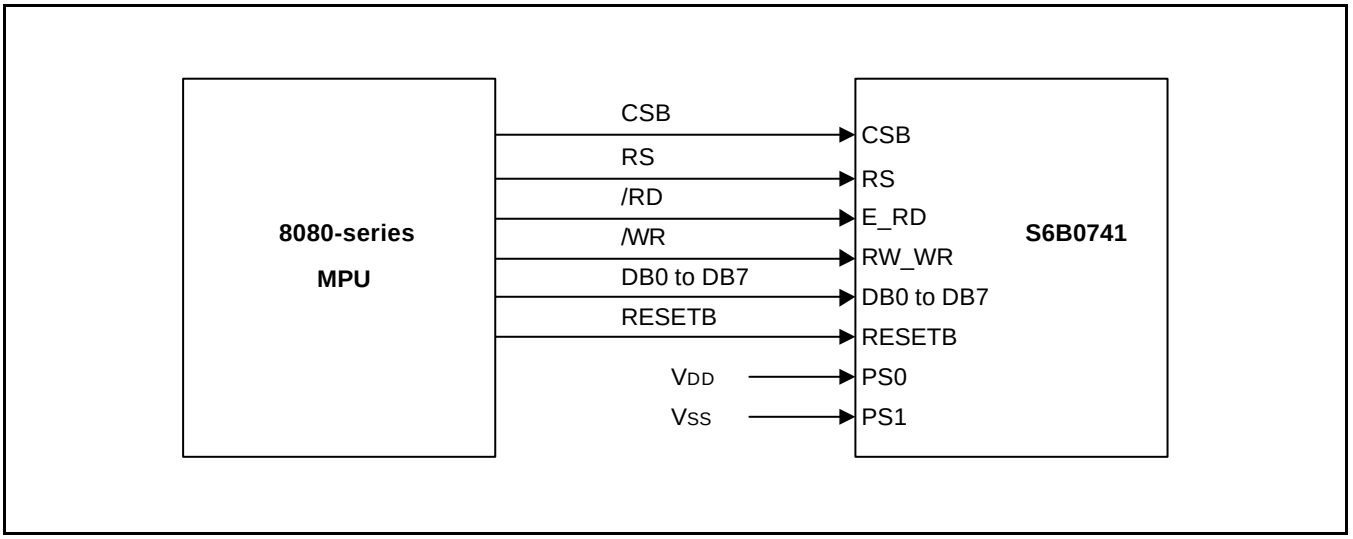

Figure 46. Interfacing with 8080-series (PS0 = "H", PS1 = "L")

In Case of 4-pin SPI mode (PS0 = "L" , PS1 = "H")

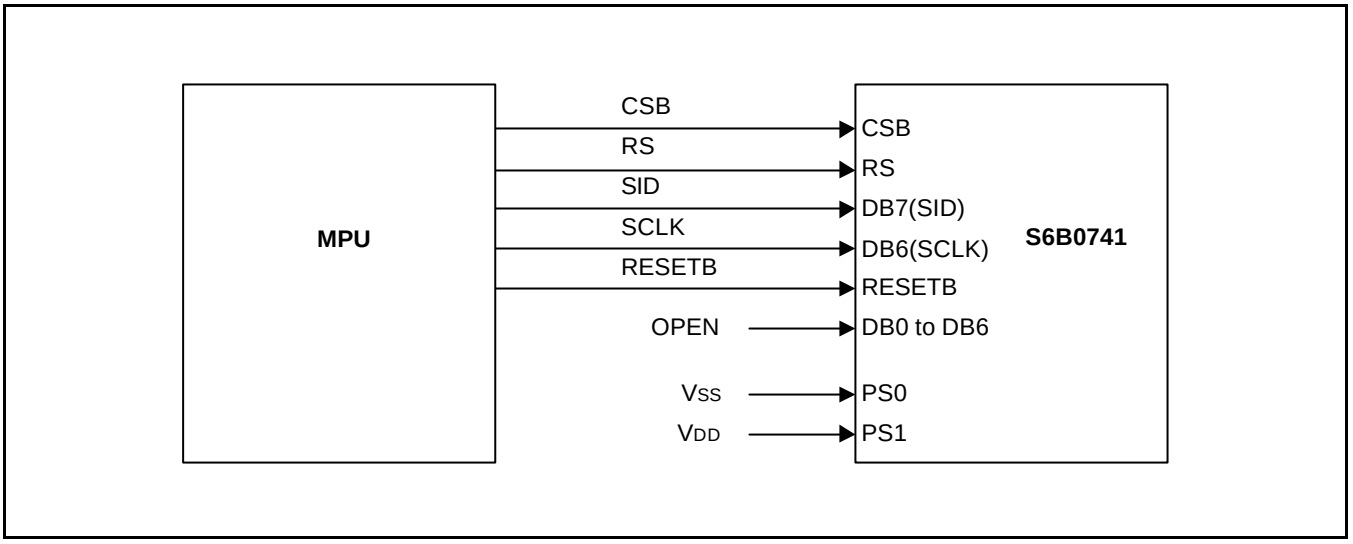

Figure 47. Serial Interface (PS0 = "L" , PS1 = "H")

In Case of 3-pin SPI mode (PS0 = "L" , PS1 = "L")

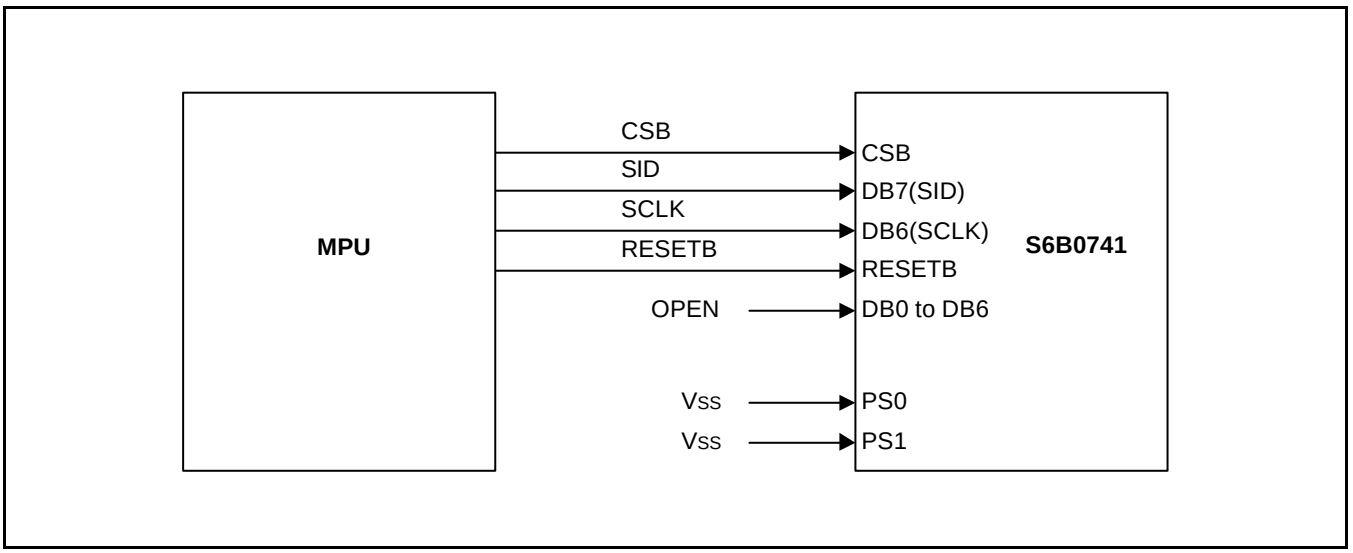

Figure 48. Serial Interface (PS0 = "L" , PS1 = "L")

CONNECTIONS BETWEEN S6B0741 AND LCD PANEL

Single Chip Configuration (1/129 Duty Configurations)

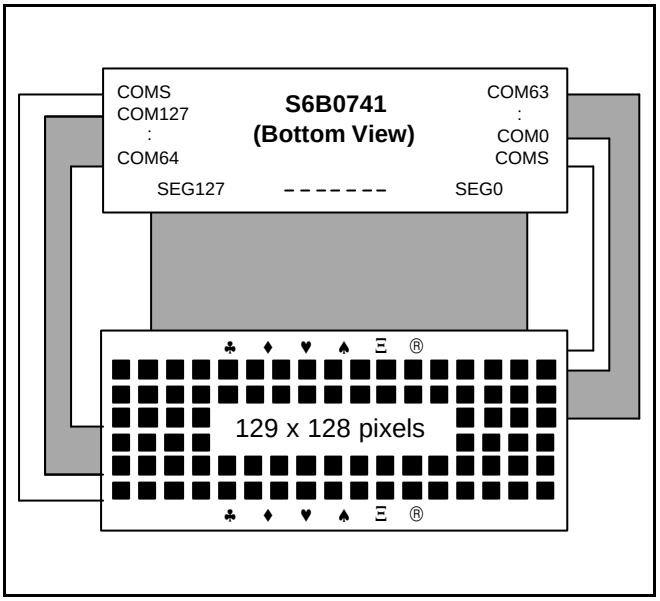

Figure 49. SHL = 0, ADC = 1

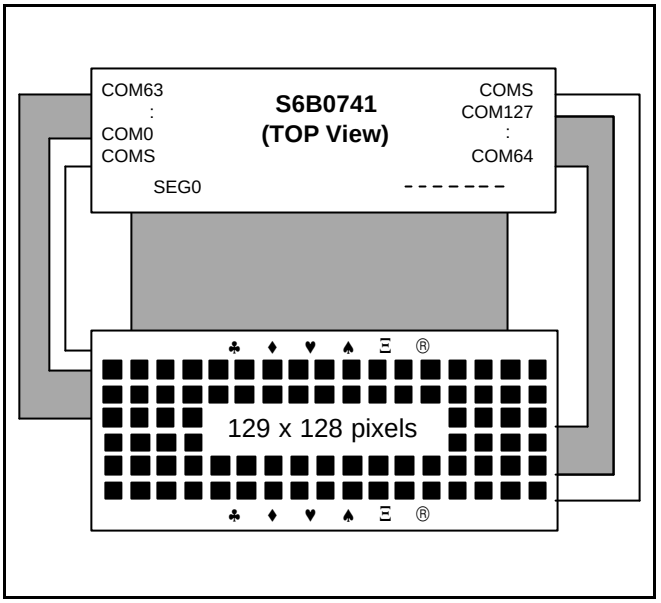

Figure 50. SHL = 0, ADC = 0

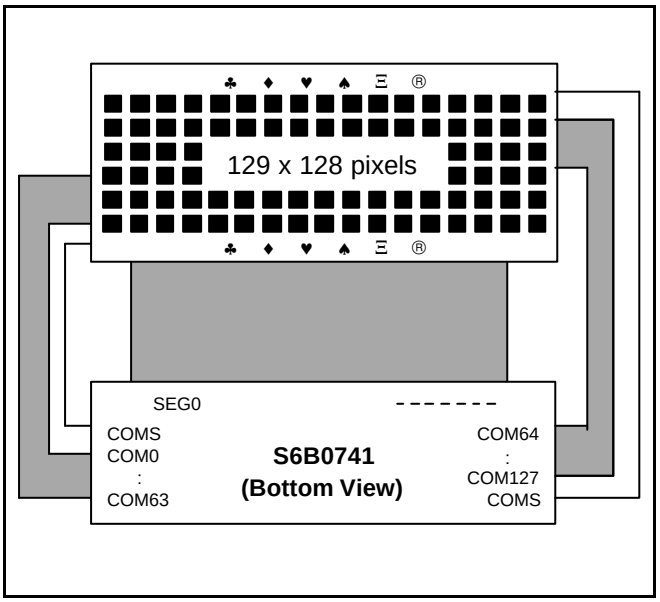

Figure 51. SHL = 1, ADC = 0

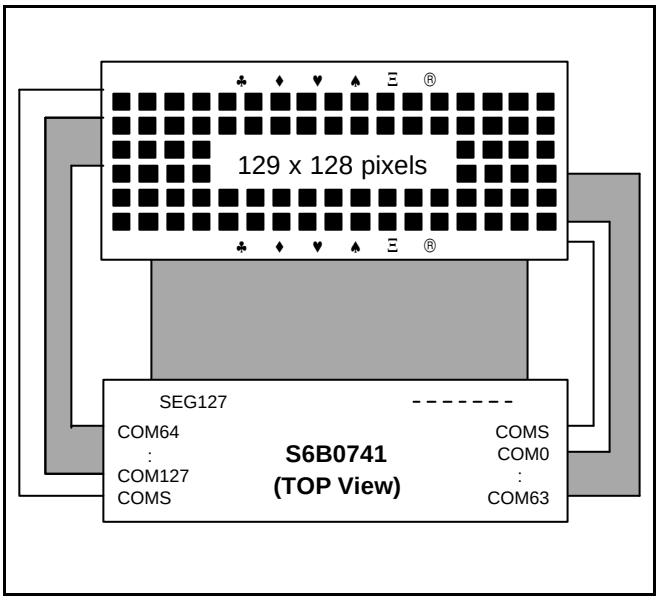

Figure 52. SHL = 1, ADC = 1

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