HCP2263 Specification

Features

- Proprietary frequency shuffling technology for improved EMI performance.
- External programmable PWM switching frequency.
- Leading edge Blanking on current sense input.
- Internal synchronized slope compensation .
- Extended burst mode control for improved efficiency and minimum standby power design
- Low VDD startup current and low operating current.
- Gate output maximum voltage clamp
- Cycle-by-Cycle Current Limiting, Built-in Adaptive Current Peak Regulation
- Power on Soft-start, Programmable CV and CC Regulation
- VDD Under Voltage Lockout with Hysteresis(UVLO),VDD OVP, VDD Clamp

Applications

- Cell Phone Charger
- Digital Cameras Charger
- Power adptor
- Set_top box power supplies
- Open_frame SMPS

Description

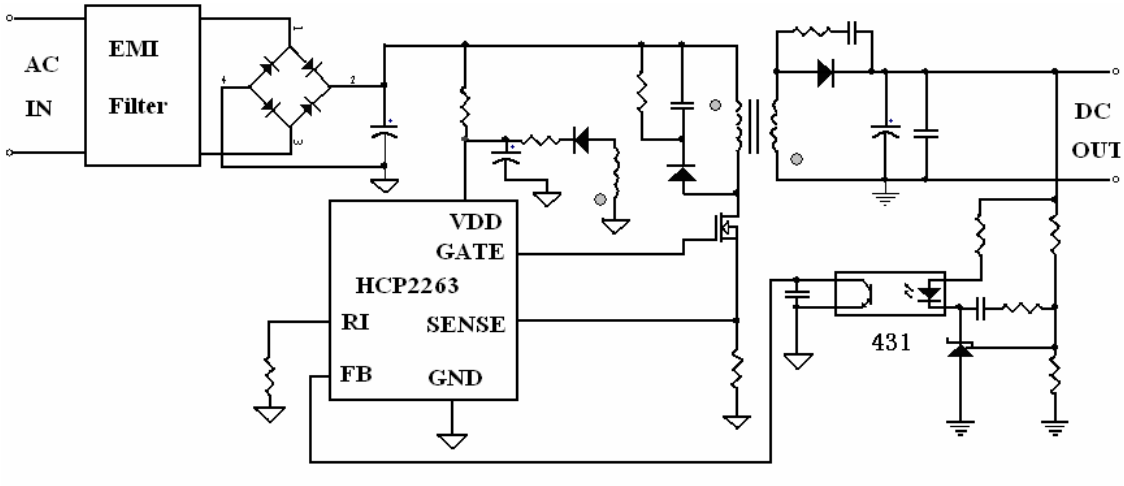
HCP2263 is highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyblack converter applications in sub 40W range.

PWM switching frequency at normal operation is externally programmable to tight range. At no load or light load condition, the IC operates in extended ‘burst mode’ to minimize switching loss.Lower standby power and higher conversion efficiency in thus achieved.

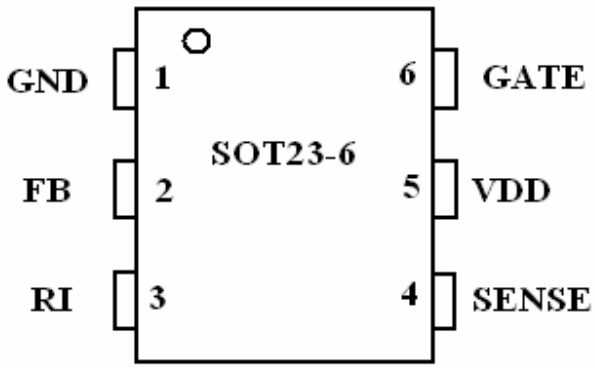
VDD low startup current and low operating current contribute to a reliable power on startup design with HCP2263.A large value resistor could thus be used in the startup circuit to minimize the standby power.

HCP2263 offers complete protection coverage with automatic self- recovery feature including Cycle-by-Cycle current limiting(OCP), over temperature protection(OTP), VDD over voltage clamp and under voltage lockout (UVLO).The Gate output is clamped to maximum 18V to protect the power MOSFET.

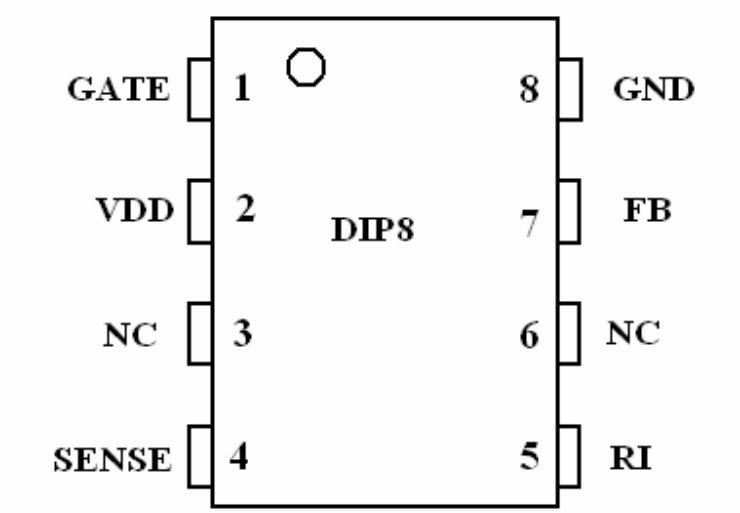
Application Circuit



Pin Assignment (SOT23-6)



Pin Assignment (DIP8)



Pin Description

Symbol	Type	Description
GATE	O	Totem-pole gate diver output for the power MOSFET
VDD	P	Chip DC power supply pin
SENSE	I	Current sense intput pin. Connected to MOSFET current resistor node.
RI	I	Internal oscillator frequency setting pin.
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and SENSE pin input.
Gnd	P	Ground.

Absolute Maximum Rating

Parameter	Value	Unit
VDD supply voltage	30	V
VDD clamp voltage	32	V
VDD clamp current	10	mA

V_{FB} input voltage	-0.3 to7	V
V_{SENSE} input voltage to SENSE pin	-0.3 to7	V
V_{RI} input voltage to RIpin	-0.3 to7	V
Min/Max operating junction temperature	-55 to 150	℃
Operating ambient temperature	-20 to 85	℃

Technical Specifications

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max	
Idd_startup	VDD start up current	VDD=12.5V RI=100K		3	10	uA
Idd	VDD current	VDD=16V RI=100KΩ, FB=3V		1.4		mA
UVLO(ON)	VDD under voltage lockout enter		7.7	8	8.8	V
UVLO(OFF)	VDD under voltage lockout exit		13.2	14	14.8	V
VDD_clamp	VDD zener clamp voltage	Idd=10mA		30		V
AVCS	PWM input gain	$\Delta V_{FB}/\Delta V_{SENSE}$		2		V/V
V_{FB}_open	V_{FB} open loop voltage			5.3		V
I_{FB}_short	FB pin short current	Short FB pin to GND and measure current		0.9		mA
V_{TH}_PL	Power limiting FB threshold voltage	Iout=－10mA		3.7		V
T_D_PL	Power limiting debounce time			32		mS
DC_MAX	Maximum duty cycle	VDD=18V,SENSE=0V RI=100KΩ,FB=3V		75		%

T_blanking	Leading edge blanking time	RI=100KΩ		250		nS
ZSENSE_IN	Input impedance			40		KΩ
VTH_sense	Over current threshold voltage			0.8		V
Fosc	Normal oscillation frequency	RI=100KΩ	60	65	70	Khz
Δf_temp	Frequency temperature stability	VD TA -20℃ to 100℃D=16V,RI=100KΩ		5		%
Δf_VDD	Frequency voltage stability	VDD=12V to 25V RI=100KΩ		5		%
RI_range	Operating RI range		50	100	150	KΩ
VRI_open	RI open load voltage			2		V
Fosc_BM	Burst mode base frequency			22		Khz
Δf_OSC	Frequency modulation range /Base frequency	RI=100KΩ	-3		+3	%
VOL	Output low level	VDD=16V,IO=-20mA			0.8	V
VOH	Output high level	VDD=16V,IO=20mA	10			V
V_Clamp	output clamp voltage level			18		V
T_r	Output rising time	VDD=16V,CL=1nF		220		nS
T_f	Output falling time	VDD=16V,CL=1nF		70		nS