# HCP2269 Specification

## Features

- Proprietary frequency shuffling technology for improved EMI performance.
- External programmable PWM switching frequency.
- Leading edge Blanking on current sense input.
- Internal synchronized slope compensation .
- Extended burst mode control for improved efficiency and minimum standby power design
- Low VDD startup current and low operating current.
- Gate output maximum voltage clamp 18V.
- Cycle-by-Cycle Current Limiting, Built-in Adaptive Current Peak Regulation
- Power on Soft-start, Programmable CV and CC Regulation
- VDD Under Voltage Lockout with Hysteresis(UVLO),VDD OVP, VDD Clamp

## Applications

- Digital Cameras Charger
- Power adaptor
- Set_top box power supplies
- Open_frame SMPS
- Battery charger

## Description

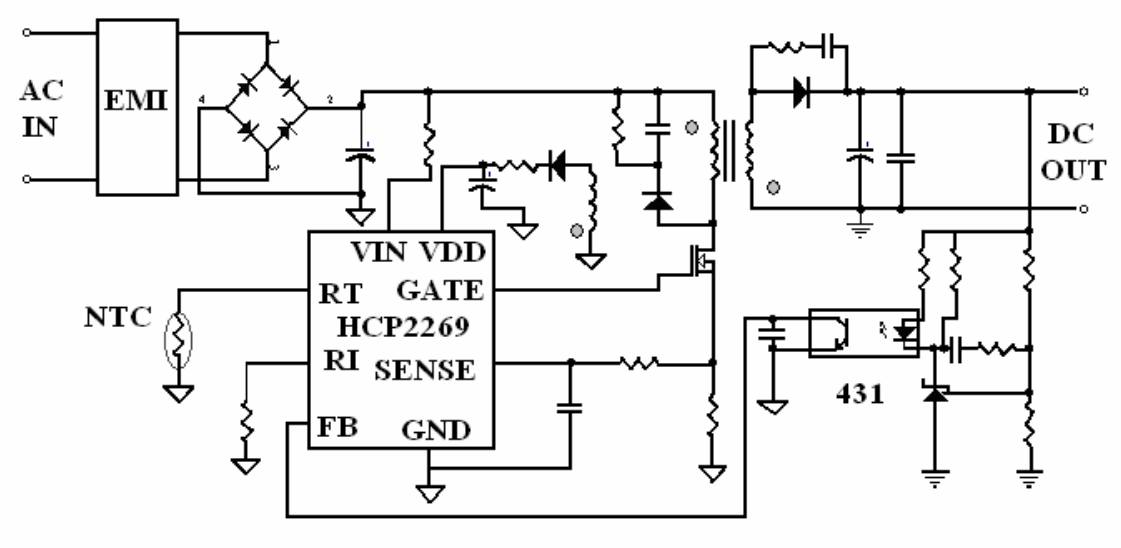
HCP2269 is highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyblack converter applications in sub 80W range.

PWM switching frequency at normal operation is externally programmable to tight range. At no load or light load condition, the IC operates in extended ‘burst mode’ to minimize switching loss.Lower standby power and higher conversion efficiency in thus achieved.

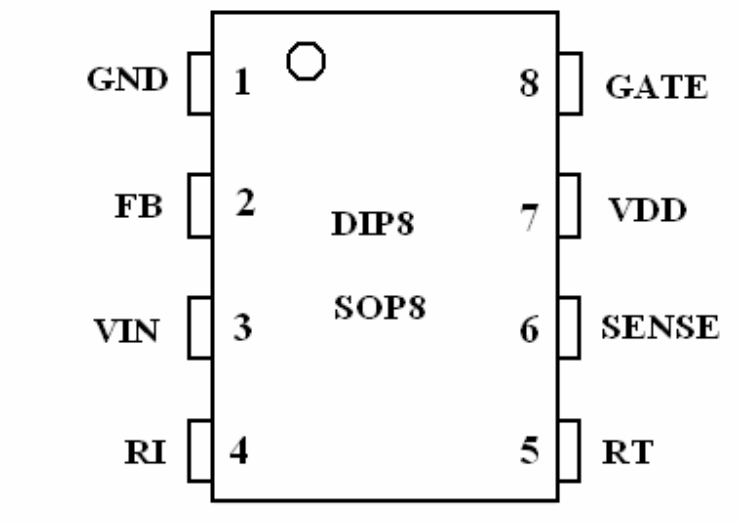
VDD low startup current and low operating current contribute to a reliable power on startup design with HCP2269.A large value resistor could thus be used in the startup circuit to minimize the standby power.

HCP2269 offers complete protection coverage with automatic self- recovery feature including Cycle-by-Cycle current limiting(OCP),over temperature protection(OTP),VDD over voltage clamp and under voltage lockout (UVLO).The Gate output is clamped to maximum 18V to protect the power MOSFET.

## Application Circuit




## Pin Assignment (DIP8,SOP8)



## Pin Description

| Symbol | Type | Description |
|---|---|---|
| GATE | O | Totem-pole gate diver output for the power MOSFET |
| VDD | P | Chip DC power supply pin |
| SENSE | I | Current sense intput pin. Connected to MOSFET current resistor node. |
| RI | I | Internal oscillator frequency setting pin. |
| FB | I | Feedback input pin.The PWM duty cycle is determined by voltage level into this pin and SENSE pin input. |
| Gnd | P | Ground. |
| RT | I | Temperature sensing intput pin,connected through a NTC resistor to GND. |
| VIN | I | Connected through a large value resistor to rectified line input for startup IC supply GND and line voltage sensing. |

## Absolute Maximum Rating

| Parameter | Value | Unit |
|---|---|---|
| VDD/VIN supply voltage | 30 | V |
| VDD zener clamp voltage | VDD clamp +0.1 | KΩ |
| VDD clamp continuous current | 10 | mA |
| $V_{FB}$ input voltage | -0.3 to 7 | V |
| $V_{SENSE}$ input voltage to SENSE pin | -0.3 to 7 | V |
| $V_{RT}$ input voltage to RT pin | -0.3 to 7 | V |
| $V_{RI}$ input voltage to RI pin | -0.3 to 7 | V |
| Operating ambient temperature | -20 to 85 | ℃ |
| Min/Max operating junction temperature | -55 to 150 | ℃ |

## Technical Specifications

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max | |
| Idd_startup | VDD start up current | VDD=12.5V<br>RI=24K | | 3 | 10 | uA |
| Idd | VDD current | VDD=18V<br>RI=24KΩ, FB=3.6V | | 2.3 | | mA |
| UVLO (enter) | VDD under voltage lockout enter | | 9.5 | 10.5 | 11.5 | V |
| UVLO(exit) | VDD under voltage lockout exit | | 15.5 | 16.5 | 17.5 | V |
| OVP(enter) | VDD over voltage protection enter | | 27 | 28 | 29 | V |
| OVP(exit) | VDD over voltage protection exit | | 25 | 26 | 27 | V |
| VDD_clamp | VDD zener clamp voltage | Idd=10mA | 29 | 30 | 31 | V |
| $T_{D}$_OVP | VDD OVP debounce time | | | 80 | | uS |
| AVCS | PWM input gain | $\Delta V_{FB}/\Delta V_{SENSE}$ | | 2.8 | | V/V |
| $V_{FB}$_open | $V_{FB}$ open loop voltage | | | 5.3 | | V |
| $I_{FB}$_short | FB pin short current | Short FB pin to GND and measure current | | 0.9 | | mA |
| $V_{TH}$_PL | Power limiting FB threshold voltage | Iout=－10mA | | 4.4 | | V |
| $T_{D}$_PL | Power limiting debounce time | | | 64 | | mS |
| DC_MAX | Maximum duty cycle | VDD=18V, FB=3V<br>SENSE=0V | | 80 | | % |
| T_blanking | Leading edge blanking time | | | 250 | | nS |

| | | | | | | |
|---|---|---|---|---|---|---|
| ZSENSE_IN | Input impedance | | | 30 | | KΩ |
| VTH_OC_0 | Current limiting threshold voltage at no compensation | I(VIN)= 0 uA | | 0.9 | | V |
| VTH_OC_1 | Current limiting threshold voltage at compensation | I(VIN)= 150 uA | | 0.81 | | V |
| Fosc | Normal oscillation frequency | RI=24KΩ | 60 | 65 | 70 | Khz |
| Δf_temp | Frequency temperature stability | TA -20℃ to 100℃ VDD=16V,RI=24KΩ | | 2 | | % |
| Δf_VDD | Frequency voltage stability | VDD=12V to 25V RI=24KΩ | | 2 | | % |
| RI_range | Operating RI range | | 12 | 24 | 60 | KΩ |
| VRI_open | RI open load voltage | | | 2 | | V |
| Fosc_BM | Burst mode base frequency | | | 22 | | Khz |
| Δf_OSC | Frequency modulation range /Base frequency | | -3 | | +3 | % |
| VOL | Output low level | VDD=18V,IO=-20mA | | | 0.3 | V |
| VOH | Output high level | VDD=18V,IO=20mA | 11 | | | V |
| V_Clamp | output clamp voltage level | | | 18 | | V |
| T_r | Output rising time | VDD=18V,CL=1nF | | 110 | | nS |
| T_f | Output falling time | VDD=18V,CL=1nF | | 40 | | nS |
| I_RT | Output current of RT pin | | | 70 | | uA |
| V_OTP | OTP threshold voltage | | 1 | 1.05 | 1.1 | V |
| V_OTP_off | OTP recovery threshold voltage | | | 1.15 | | V |
| T_OTP | OTP de-bounce time | | | 100 | | uS |